GANDHI SCHOOL OF ENGINEERING

BHABANDHA, BERHAMPUR

BRANCH:- ELECTRICAL ENGINEERING

SEMESTER:- 5TH

SUBJECT:- DEMP

Name of the Faculty-Er. P.P MAHUNTA & Er. LALIT NAYAK

Sl. No	Topic/Module	No. of period	Topic to be taken		Topic No.	Actual topictaken		Remarks
			Details of the topics	Date		Topic Name	Date	
1	BASICS OF DIGITAL ELECTRONICS	15	1.1 Binary, Octal, Hexadecimal number systems and compare with Decimal system. 1.2 Binary addition, subtraction, Multiplication and Division. 1.3 1's complement and 2's complement numbers for a binary number 1.4 Subtraction of binary numbers in 2's complement method. 1.5 Use of weighted and Un-weighted codes & write Binary equivalent number for a number in 8421, Excess-3 and Gray Code and vice-versa. 1.6 Importance of parity Bit. 1.7 Logic Gates: AND, OR, NOT, NAND, NOR and EX-OR gates with truth table.	20.09.2022 TO 20.10.2022	1.1 1.2 1.3 1.4 1.5 1.6 1.7 1.8 1.9	Binary, Octal, Hexadecimal number systems and compare with Decimal system. Binary addition, subtraction, Multiplication and Division. 1's complement and 2's complement numbers for a binary number Subtraction of binary numbers in 2's complement method. Use of weighted and Un-weighted codes & write Binary equivalent number for a number in 8421, Excess-3 and Gray Code and	20.09.2022 21.09.2022 23.09.2022 24.09.2022 26.09.2022 27.09.2022 29.09.2022 30.09.2022 11.10.2022 13.10.2022 14.10.2022 17.10.2022 18.10.2022 19.10.2022 20.10.2022	

			1.8 Realize AND, OR, NOT operations using NAND, NOR gates. 1.9 Different postulates and De-Morgan's theorems in Boolean algebra. 1.10 Use Of Boolean Algebra For Simplification Of Logic Expression 1.11 Karnaugh Map For 2,3,4 Variable, Simplification Of SOP And POS Logic Expression Using K-Map.		**1.10** **1.11**	vice-versa. Importance of parity Bit. Logic Gates: AND, OR, NOT, NAND, NOR and EX-OR gates with truth table. Realize AND, OR, NOT operations using NAND, NOR gates. Different postulates and De-Morgan's theorems in Boolean algebra. Use Of Boolean Algebra For Simplification Of Logic Expression Karnaugh Map For 2,3,4 Variable, Simplification Of SOP And POS Logic Expression Using K-Map.	
2	**COMBINATIONAL LOGIC CIRCUITS**	**15**	2.1 Give the concept of combinational logic circuits. 2.2 Half adder circuit and verify its functionality using truth table. 2.3 Realize a Half-adder using NAND gates only and NOR gates only. 2.4 Full adder circuit and explain its operation with truth table. 2.5 Realize full-adder using two Half-adders and an OR – gate and write truth table 2.6 Full subtractor circuit and explain its operation with truth table. 2.7 Operation of 4 X 1 Multiplexers and 1 X 4 demultiplexer 2.8 Working of Binary-Decimal Encoder	**21.10.2022 TO 18.11.2022**	**2.1** **2.2** **2.3** **2.4** **2.5** **2.6** **2.7** **2.8** **2.9**	Give the concept of combinational logic circuits. Half adder circuit and verify its functionality using truth table. Realize a Half-adder using NAND gates only and NOR gates only. Full adder circuit and explain its operation with truth table. Realize full-adder using two Half-adders and an OR – gate and write truth table Full subtractor circuit and explain its operation with	**21.10.2022 22.10.2022 23.10.2022 26.10.2022 27.10.2022 28.10.2022 30.10.2022 01.11.2022 02.11.2022 03.11.2022 04.11.2022 07.11.2022 08.11.2022 10.11.2022**	

			& 3 X 8 Decoder. 2.9 Working of Two bit magnitude comparator.				truth table. Operation of 4 X 1 Multiplexers and 1 X 4 demultiplexer Working of Binary-Decimal Encoder & 3 X 8 Decoder. Working of Two bit magnitude comparator.	**11.11.2022** **14.11.2022** **15.11.2022** **17.11.2022** **18.11.2022**	
3	**SEQUENTIAL LOGIC CIRCUITS**	**15**	3.1 Give the idea of Sequential logic circuits. 3.2 State the necessity of clock and give the concept of level clocking and edge triggering, 3.3&3.4 Clocked SR flip flop with preset and clear inputs. 3.5 Construct level clocked JK flip flop using S-R flip-flop and explain with truth table 3.6 Concept of race around condition and study of master slave JK flip flop. 3.7 Give the truth tables of edge triggered D and T flip flops and draw their symbols. 3.8 Applications of flip flops. 3.9 Define modulus of a counter 3.10 4-bit asynchronous counter and its timing diagram. 3.11 Asynchronous decade counter. 3.12 4-bit synchronous counter. 3.13 Distinguish between synchronous and asynchronous counters. 3.14 State the need for a Register and	**19.11.2022 TO 10.12.2022**	**3.1** **3.2** **3.3** **3.4** **3.5** **3.6** **3.7** **3.9** **3.10** **3.11** **3.12** **3.13** **3.14** **3.15**		Give the idea of Sequential logic circuits. State the necessity of clock and give the concept of level clocking and edge triggering, Clocked SR flip flop with preset and clear inputs. Construct level clocked JK flip flop using S-R flip-flop and explain with truth table Concept of race around condition and study of master slave JK flip flop. Give the truth tables of edge triggered D and T flip flops and draw their symbols. Applications of flip flops. Define modulus of a counter 4-bit asynchronous counter and its timing diagram. Asynchronous decade counter. 4-bit synchronous counter.	**19.11.2022** **21.11.2022** **25.11.2022** **02.12.2022** **03.12.2022** **05.12.2022** **07.12.2022** **08.12.2022** **09.12.2022** **10.12.2022**	

			list the four types of registers. 3.15 Working of SISO, SIPO, PISO, PIPO Register with truth table using flip flop.			Distinguish between synchronous and asynchronous counters. State the need for a Register and list the four types of registers. Working of SISO, SIPO, PISO, PIPO Register with truth table using flip flop.		
4	8085 MICROPROCESSOR	20	4.1 Introduction to Microprocessors, Microcomputers 4.2 Architecture of Intel 8085A Microprocessor and description of each block. 4.3 Pin diagram and description. 4.4 Stack, Stack pointer & stack top 4.5 Interrupts 4.6 Opcode & Operand, 4.7 Differentiate between one byte, two byte & three byte instruction with example. 4.8 Instruction set of 8085 example 4.9 Addressing mode 4 .10 Fetch Cycle, Machine Cycle, Instruction Cycle, T-State 4.11 Timing Diagram for memory read, memory write, I/O read, I/O write 4.12 Timing Diagram for 8085 instruction 4.13 Counter and time delay. 4. 14 Simple assembly language programming of 8085.	12.12.2022 TO 17.12.2022	4.1 4.2 4.3 4.4 4.5 4.6 4.7 4.8 4.9 4.10 4.11 4.12 4.13 4.14	Introduction to Microprocessors, Microcomputers Architecture of Intel 8085A Microprocessor and description of each block. Pin diagram and description. Stack, Stack pointer & stack top Interrupts Opcode & Operand, Differentiate between one byte, two byte & three byte instruction with example. 4.8 Instruction set of 8085 example Addressing mode Fetch Cycle, Machine Cycle, Instruction Cycle, T-State Timing Diagram for memory read, memory write, I/O read, I/O write Timing Diagram for 8085 instruction Counter and time delay.	12.12.2022 14.12.2022 15.12.2022 16.12.2022 17.12.2022	

							Simple assembly language programming of 8085.	
5	**INTERFACING AND SUPPORT CHIPS**	**10**	5.1 Basic Interfacing Concepts, Memory mapping & I/O mapping 5.2 Functional block diagram and description of each block of Programmable peripheral interface Intel 8255 , 5.3 Application using 8255: Seven segment LED display, Square wave generator, Traffic light Controller	**19.12.2022 TO 10.01.2023**	**5.1** **5.2** **5.3**	Basic Interfacing Concepts, Memory mapping & I/O mapping Functional block diagram and description of each block of Programmable peripheral interface Intel 8255 , Application using 8255: Seven segment LED display, Square wave generator, Traffic light Controller	**19.12.2022** **21.12.2022** **22.12.2022** **23.12.2022** **04.01.2023** **05.01.2023** **07.01.2023** **09.01.2023** **10.01.2023**	

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