



**GANDHI SCHOOL OF
ENGINEERING, BHABANDHA, BERHAMPUR**

TEACHING AND LEARNING MATERIAL

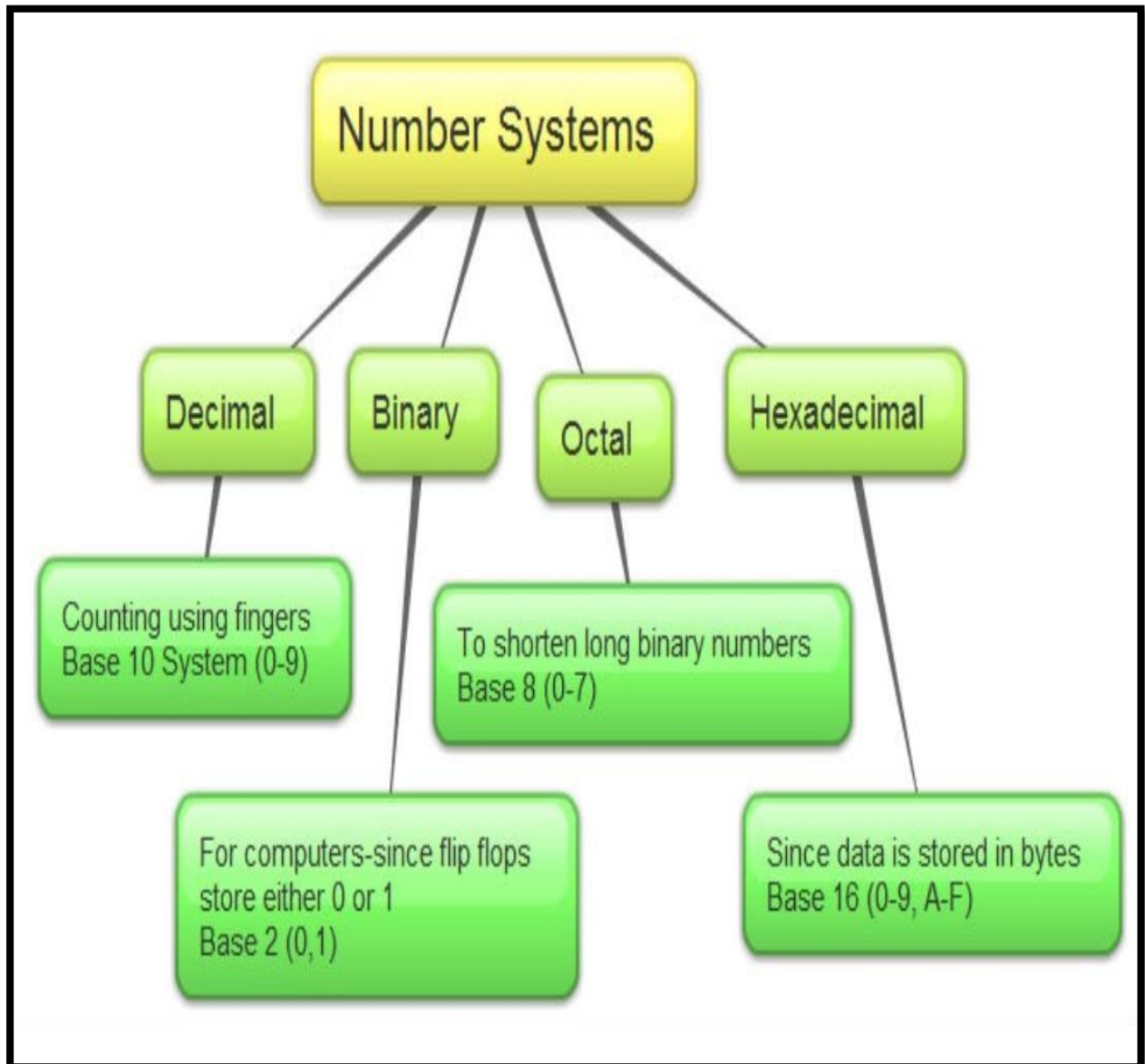
**SUBJECT: DIGITAL ELECTRONICS &
MICROPROCESSOR
SEMESTER: 5TH**

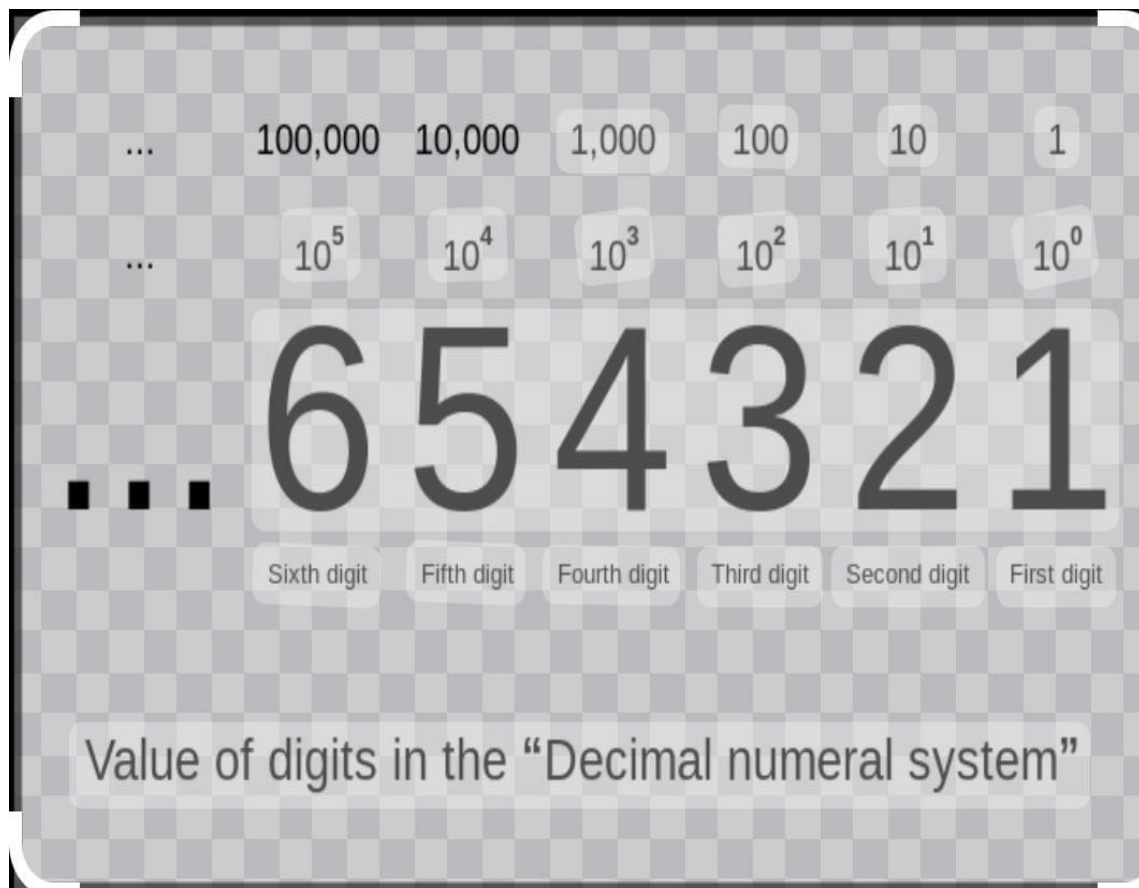
SUBMITTED BY:-

ER. LALIT NAYAK & ER. PRAGYAN PARMITA MAHUNTA

UNIT-1

NUMBER SYSTEM & CODES





Binary Number	1	0	1	1	0	1	Decimal Number
Power of base	2^5	2^4	2^3	2^2	2^1	2^0	45
Decimal equivalent	32	16	8	4	2	1	
Magnitude of each term	32	0	8	4	0	1	

Octal Number System

- The base is 8.
- Symbols : 0, 1, 2, 3, 4, 5, 6, and 7.
- Positional weights :

$$8^0 = 1$$

$$8^{-1} = 1/8$$

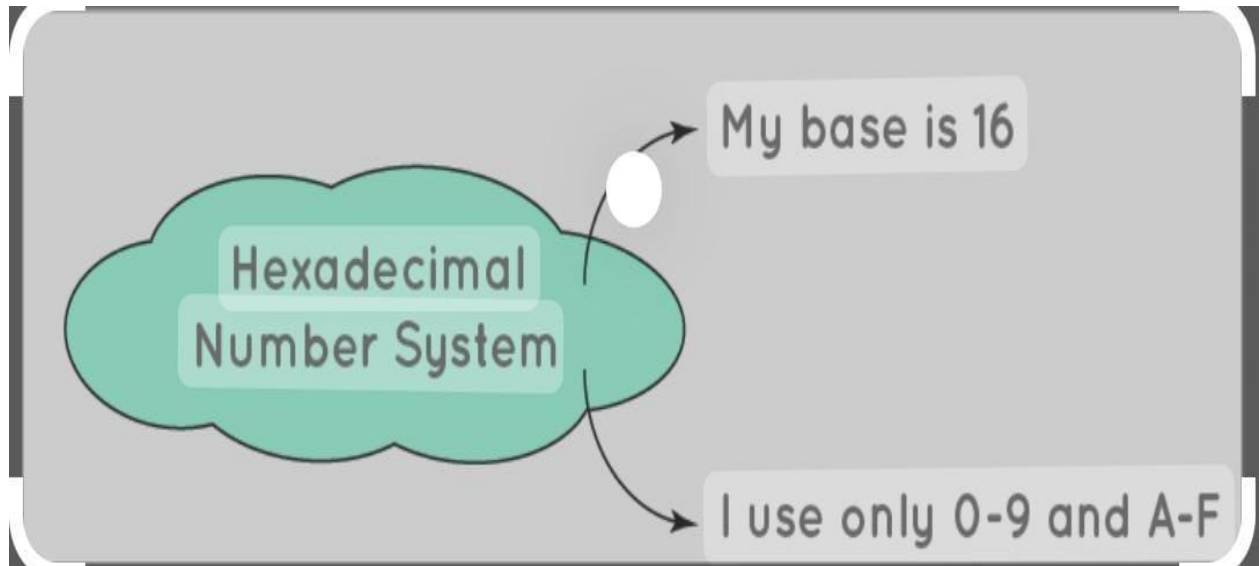
$$8^1 = 8$$

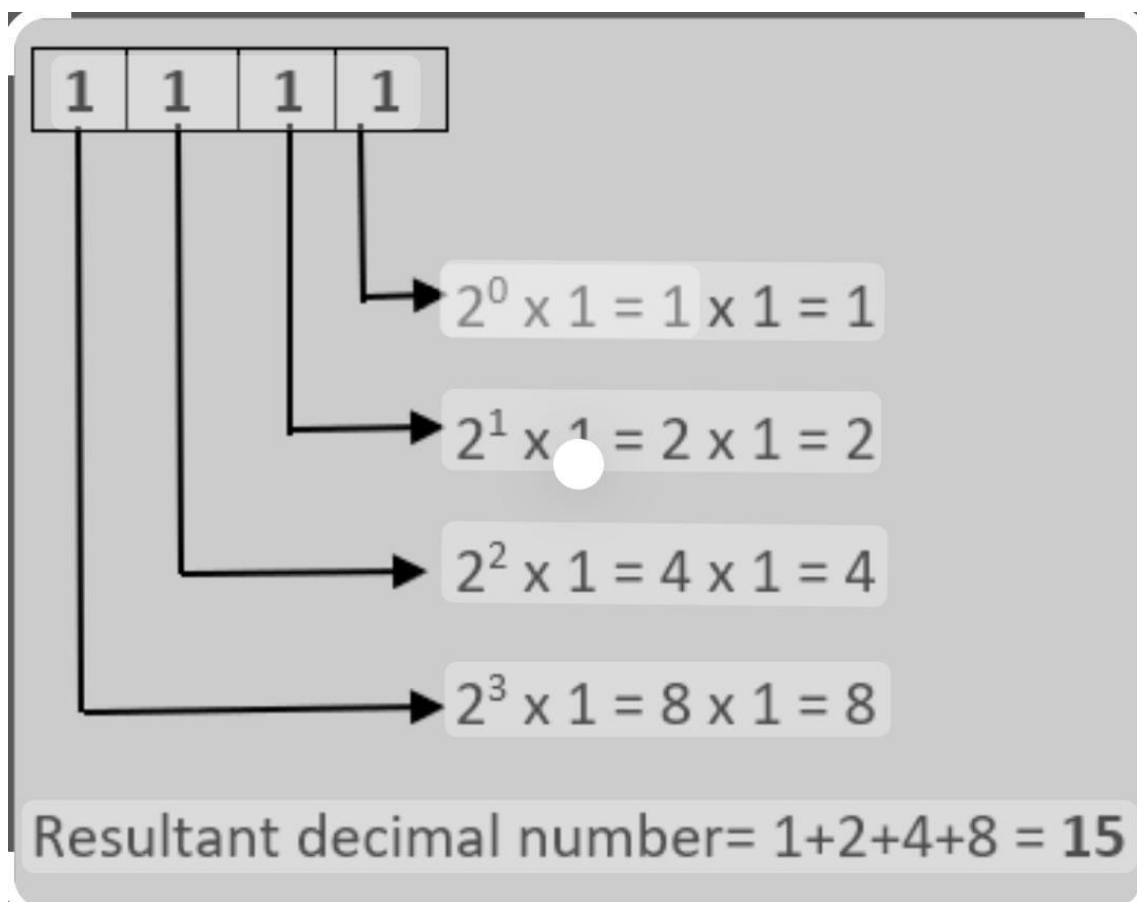
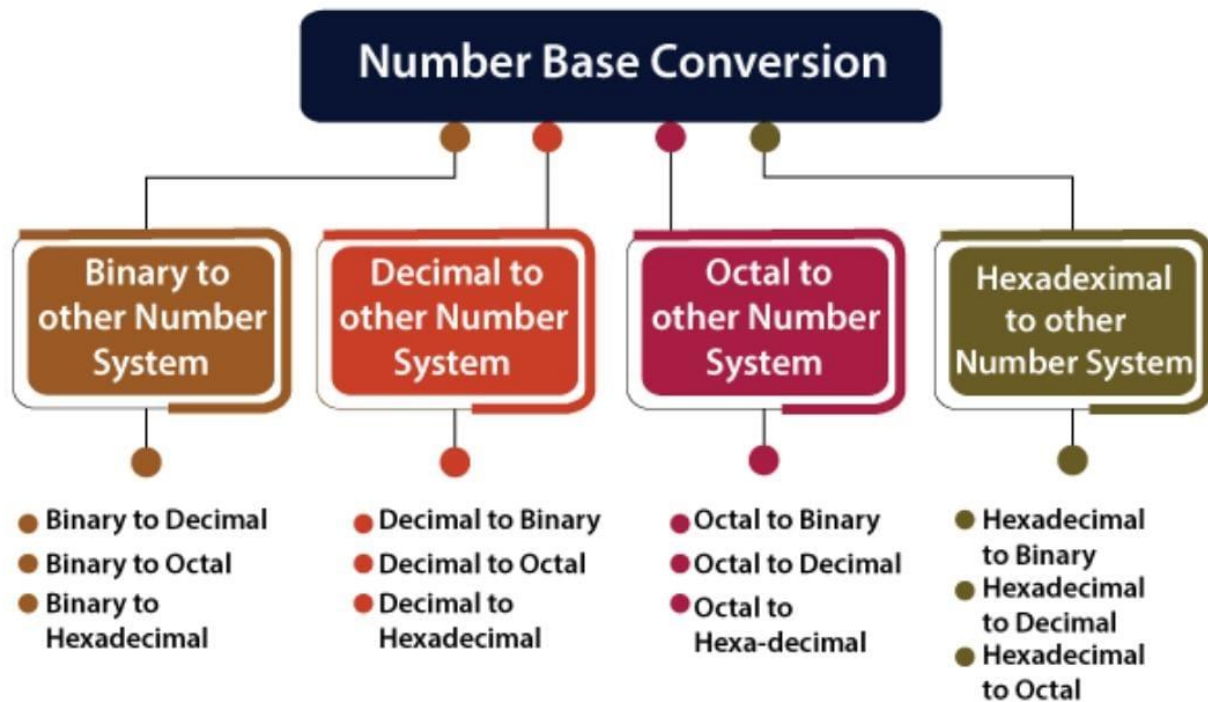
$$8^{-2} = 1/64$$

$$8^2 = 64$$

$$8^{-3} = 1/256$$

$$8^3 = 256$$





OCTAL	BINARY
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

Binary to Octal

Hexadecimal	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Decimal	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Binary Value = **010101**

0 1 0

$2^2 \quad 2^1 \quad 2^0$

$4 \times 0 \quad 2 \times 1 \quad 1 \times 0$

0 + 2 + 1

2

1 0 1

$2^2 \quad 2^1 \quad 2^0$

$4 \times 1 \quad 2 \times 0 \quad 1 \times 1$

4 + 0 + 1









5

$(10101)_2 = (25)_8$

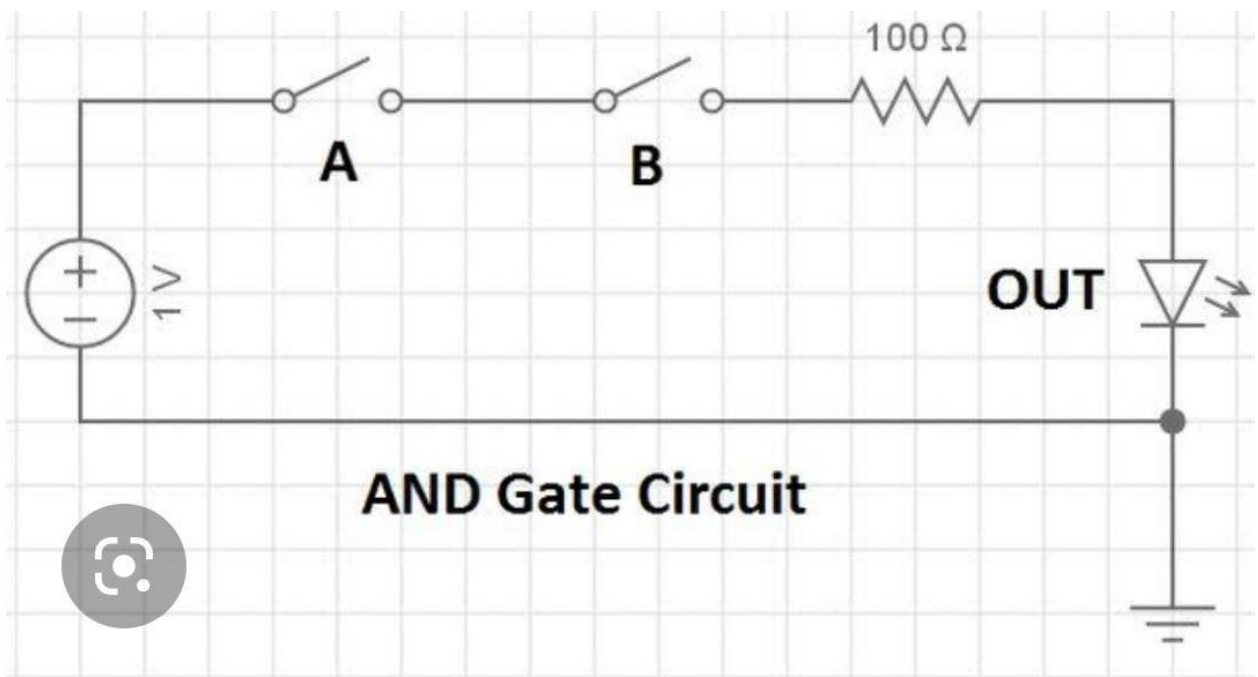
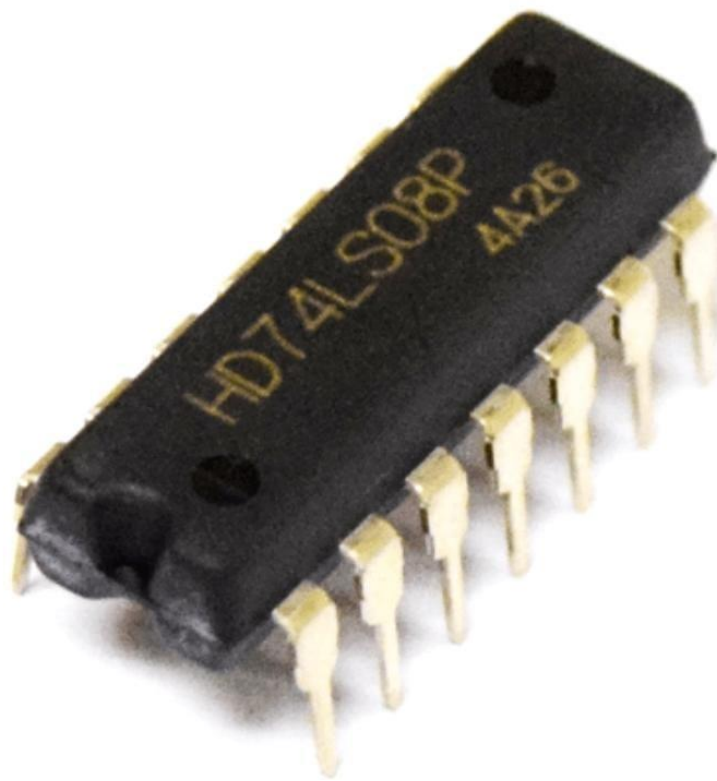
Decimal	Binary	Hexadecimal
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F

1110011100010000

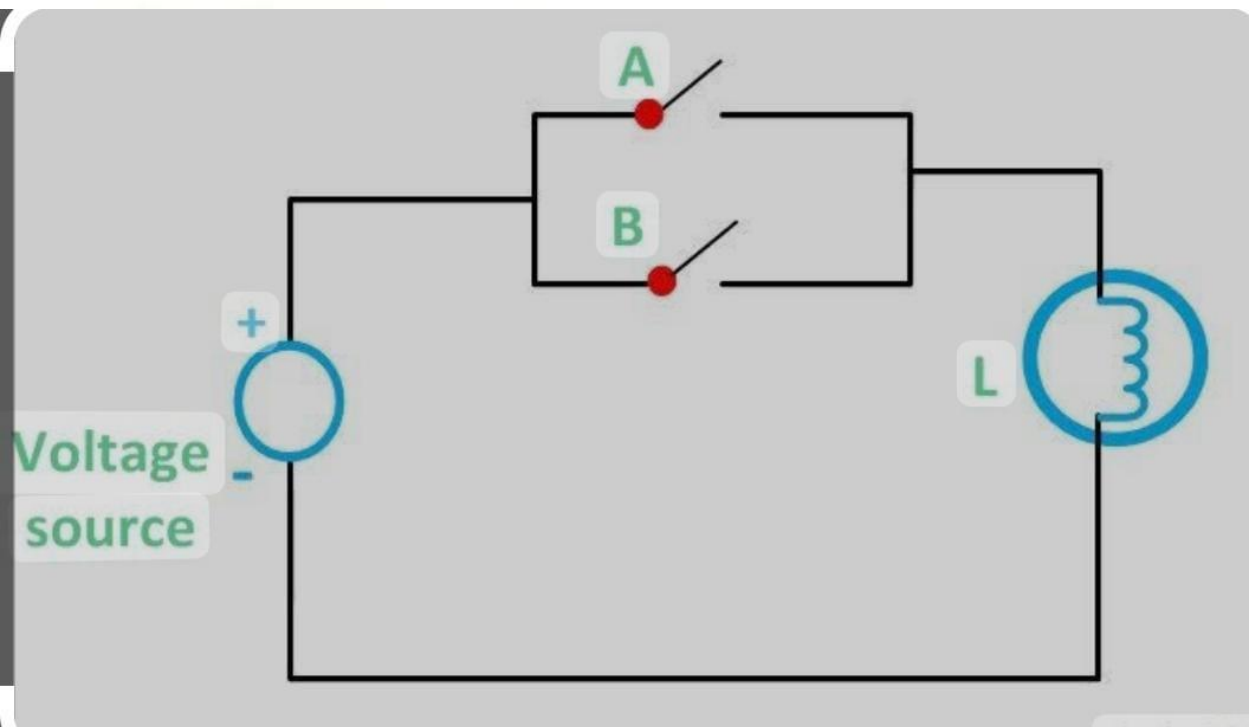
E710

Name	Graphic symbol	Algebraic function	Truth table															
AND		$F = x \cdot y$	<table><tr><th>x</th><th>y</th><th>F</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	x	y	F	0	0	0	0	1	0	1	0	0	1	1	1
x	y	F																
0	0	0																
0	1	0																
1	0	0																
1	1	1																
OR		$F = x + y$	<table><tr><th>x</th><th>y</th><th>F</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	x	y	F	0	0	0	0	1	1	1	0	1	1	1	1
x	y	F																
0	0	0																
0	1	1																
1	0	1																
1	1	1																
Inverter		$F = x'$	<table><tr><th>x</th><th>F</th></tr><tr><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td></tr></table>	x	F	0	1	1	0									
x	F																	
0	1																	
1	0																	
Buffer		$F = x$	<table><tr><th>x</th><th>F</th></tr><tr><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td></tr></table>	x	F	0	0	1	1									
x	F																	
0	0																	
1	1																	
NAND		$F = (xy)'$	<table><tr><th>x</th><th>y</th><th>F</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	x	y	F	0	0	1	0	1	1	1	0	1	1	1	0
x	y	F																
0	0	1																
0	1	1																
1	0	1																
1	1	0																
NOR		$F = (x + y)'$	<table><tr><th>x</th><th>y</th><th>F</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	x	y	F	0	0	1	0	1	0	1	0	0	1	1	0
x	y	F																
0	0	1																
0	1	0																
1	0	0																
1	1	0																
Exclusive-OR (XOR)		$F = xy' + x'y$ $= x \oplus y$	<table><tr><th>x</th><th>y</th><th>F</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	x	y	F	0	0	0	0	1	1	1	0	1	1	1	0
x	y	F																
0	0	0																
0	1	1																
1	0	1																
1	1	0																
Exclusive-NOR or equivalence		$F = xy + x'y'$ $= (x \oplus y)'$	<table><tr><th>x</th><th>y</th><th>F</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	x	y	F	0	0	1	0	1	0	1	0	0	1	1	1
x	y	F																
0	0	1																
0	1	0																
1	0	0																
1	1	1																

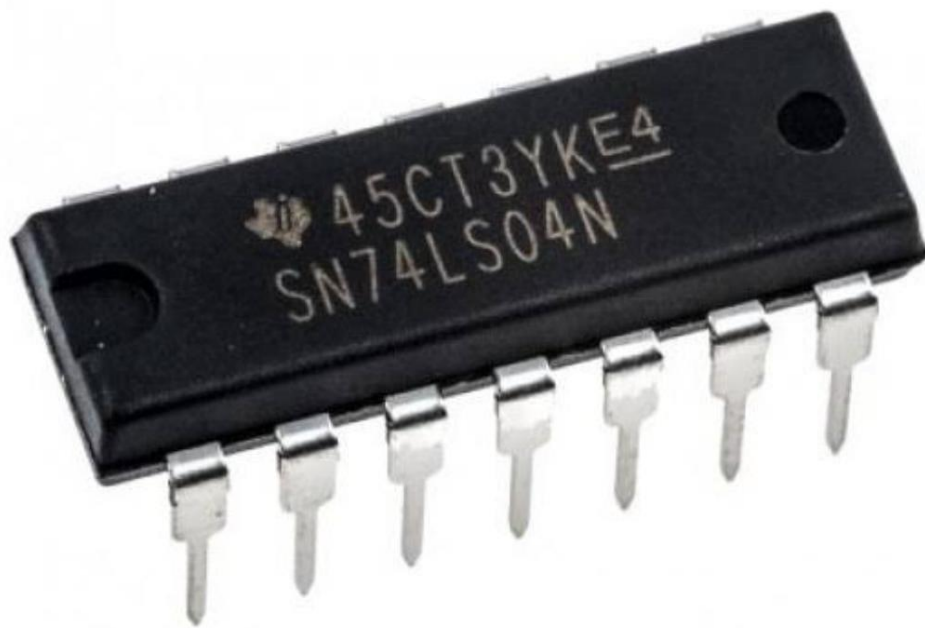
2-input AND gate



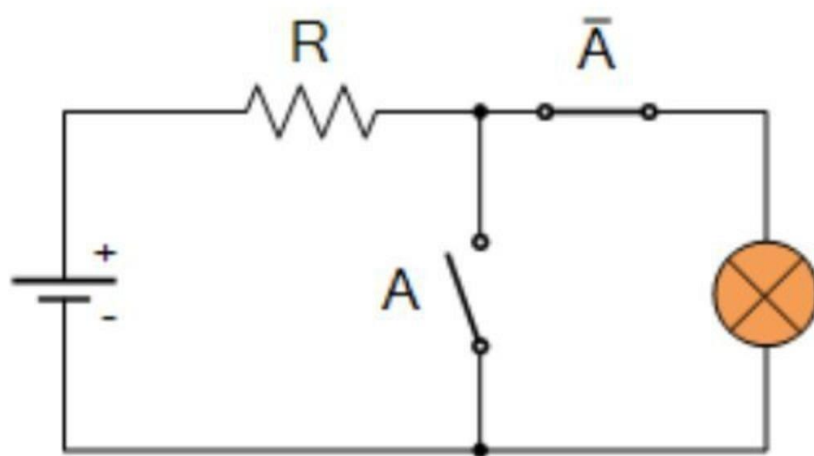
2-input OR gate



NOT gate

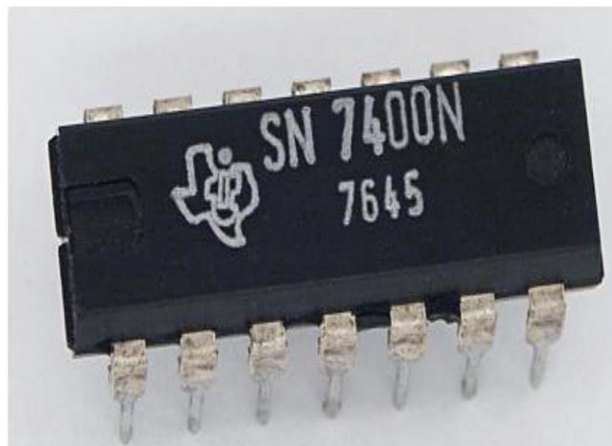
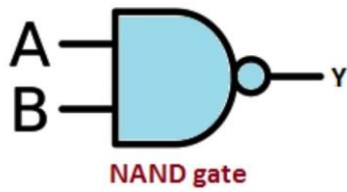
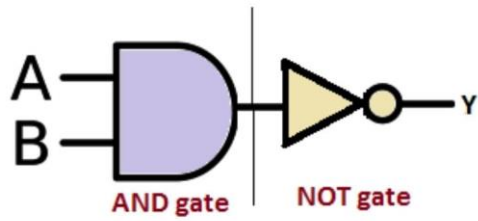


NOT Gate

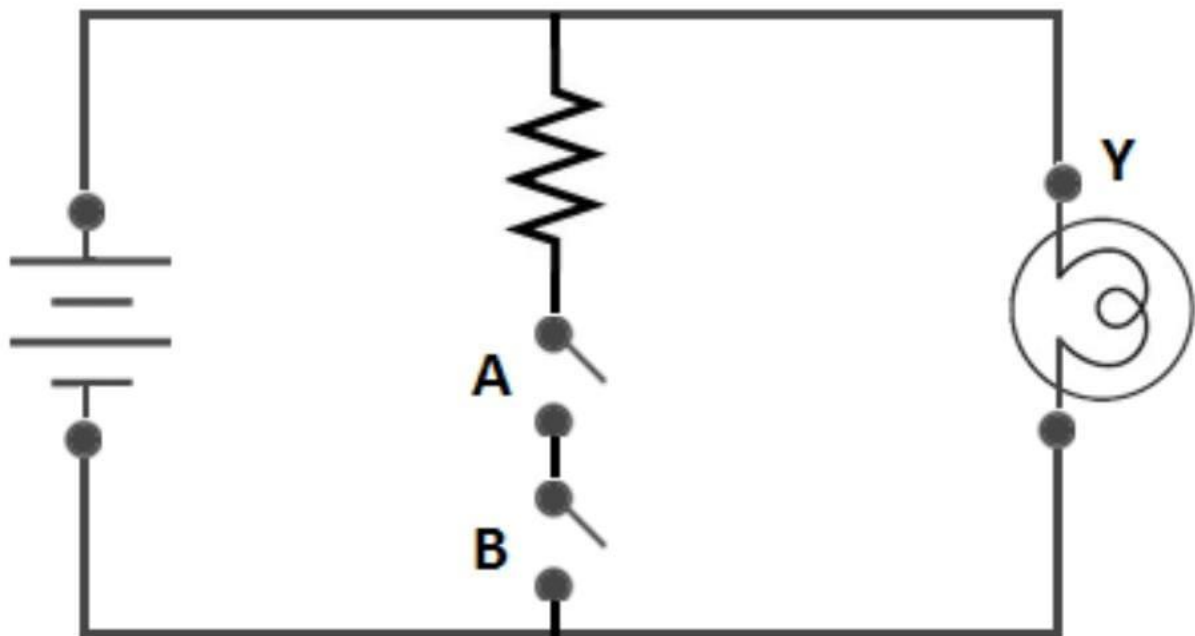


Switch A - Open = "0", Lamp - ON = "1"
 Switch A - Closed = "1", Lamp - OFF = "0"

NAND GATE



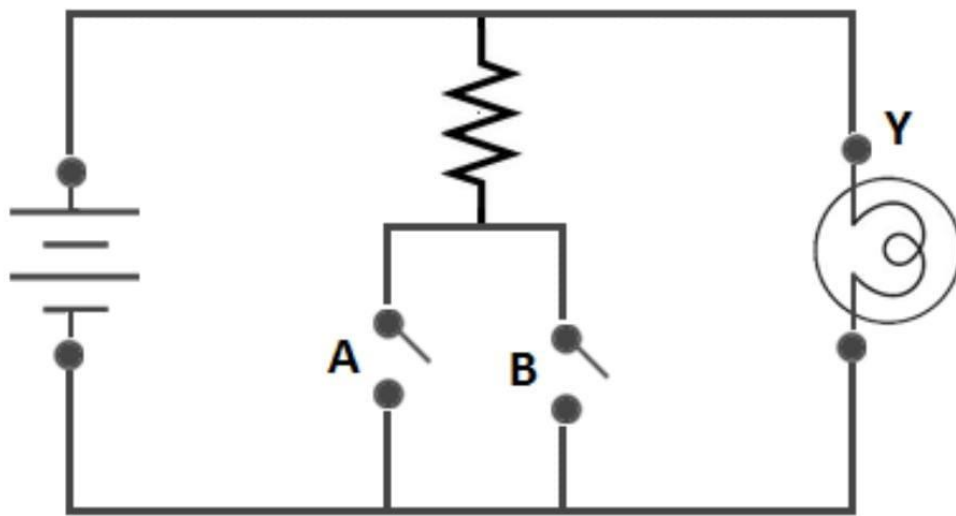
NAND GATE



Electrical Circuit

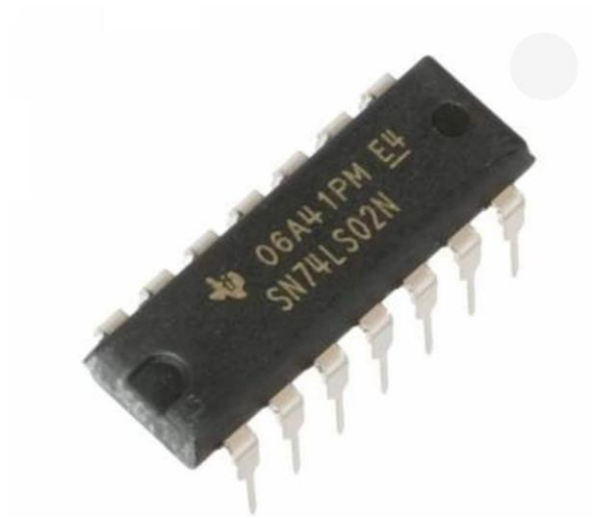
NOR GATE

NOR GATE

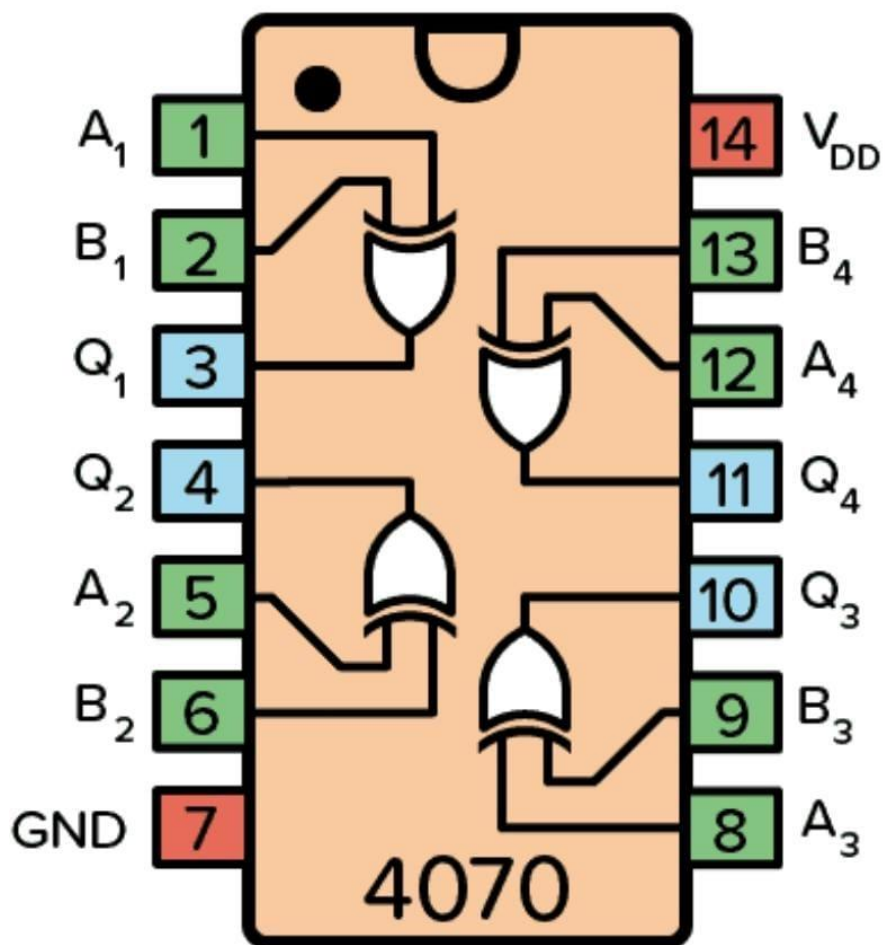
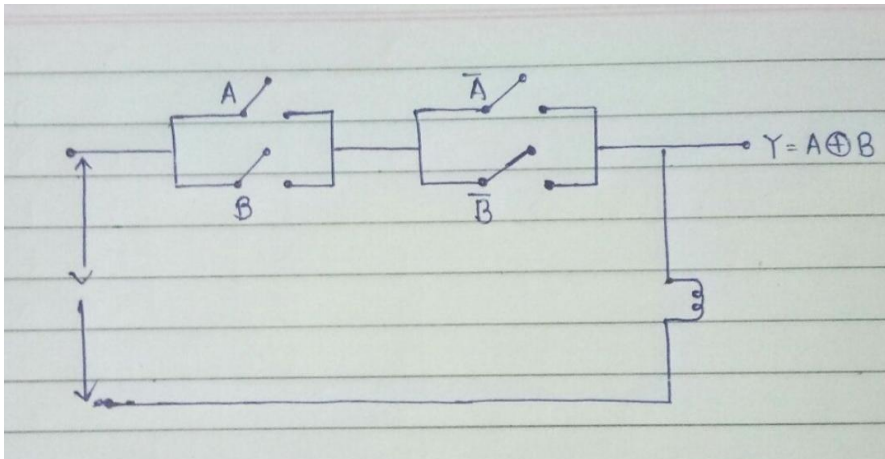


Electrical Circuit

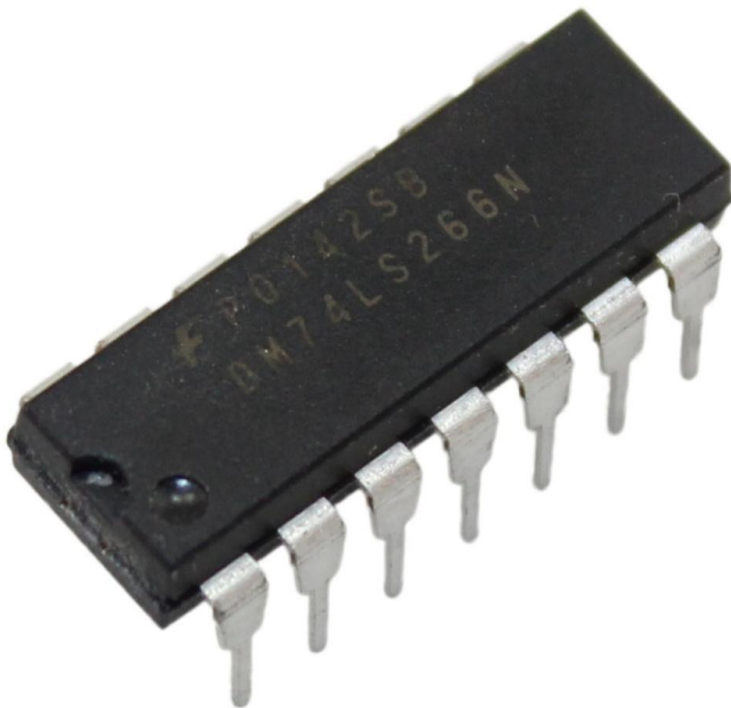
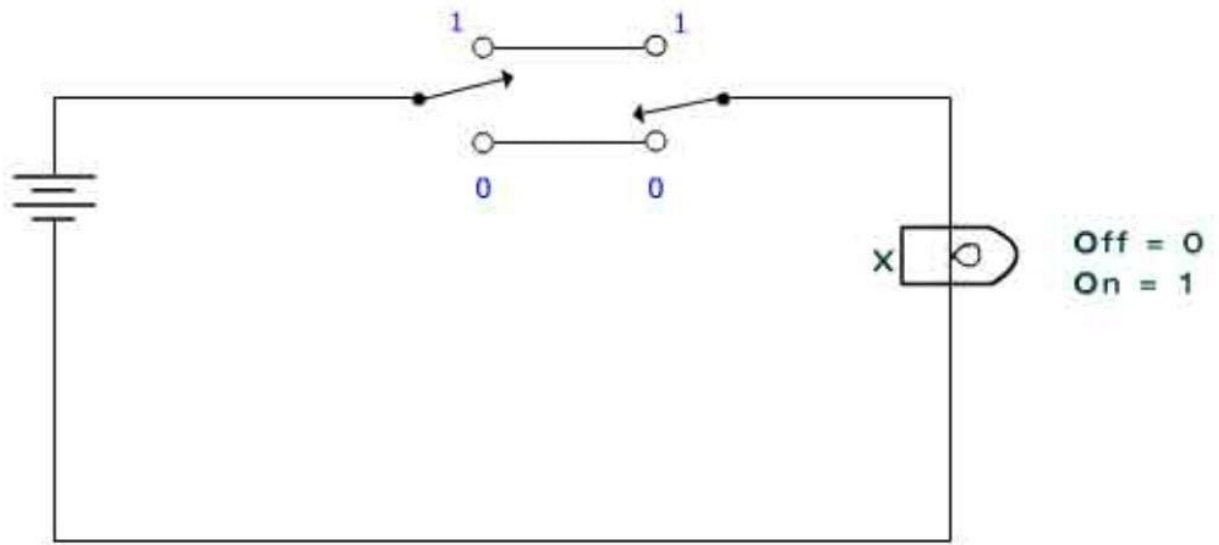
NOR Gate DIP14



EX-OR GATE



EX-NOR GATE

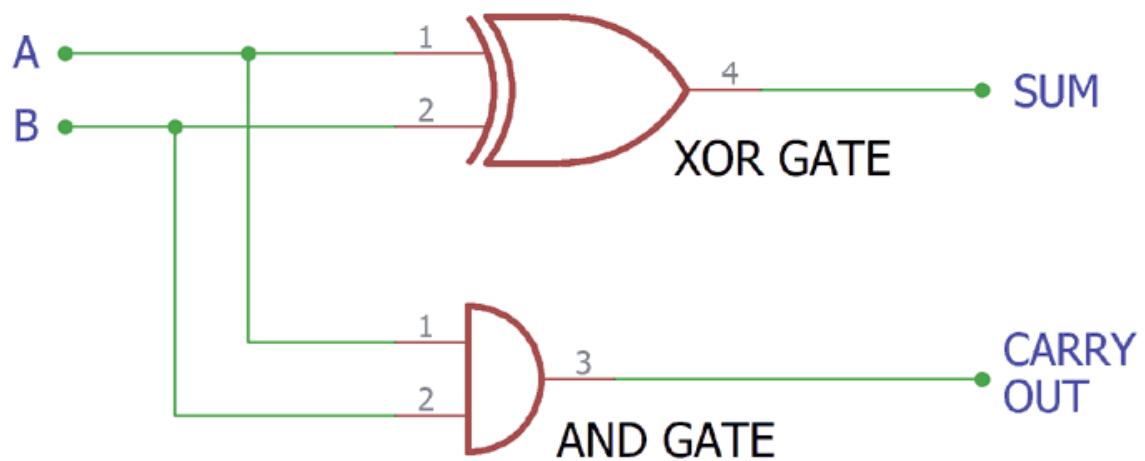


UNIT-2

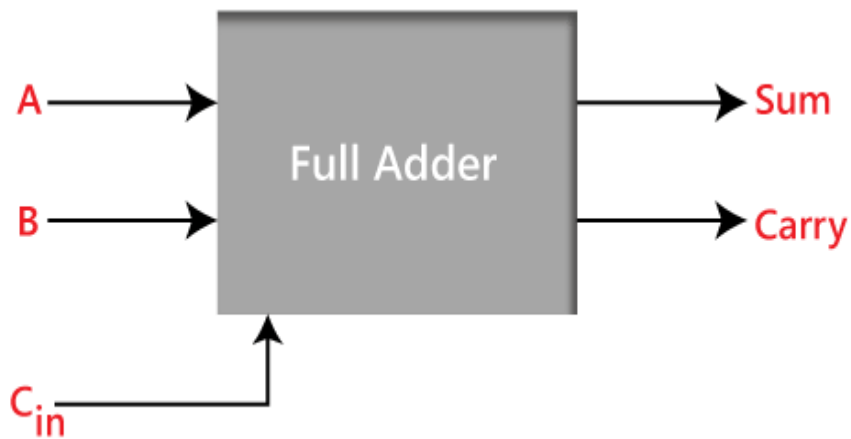
COMBINATIONAL CIRCUITS



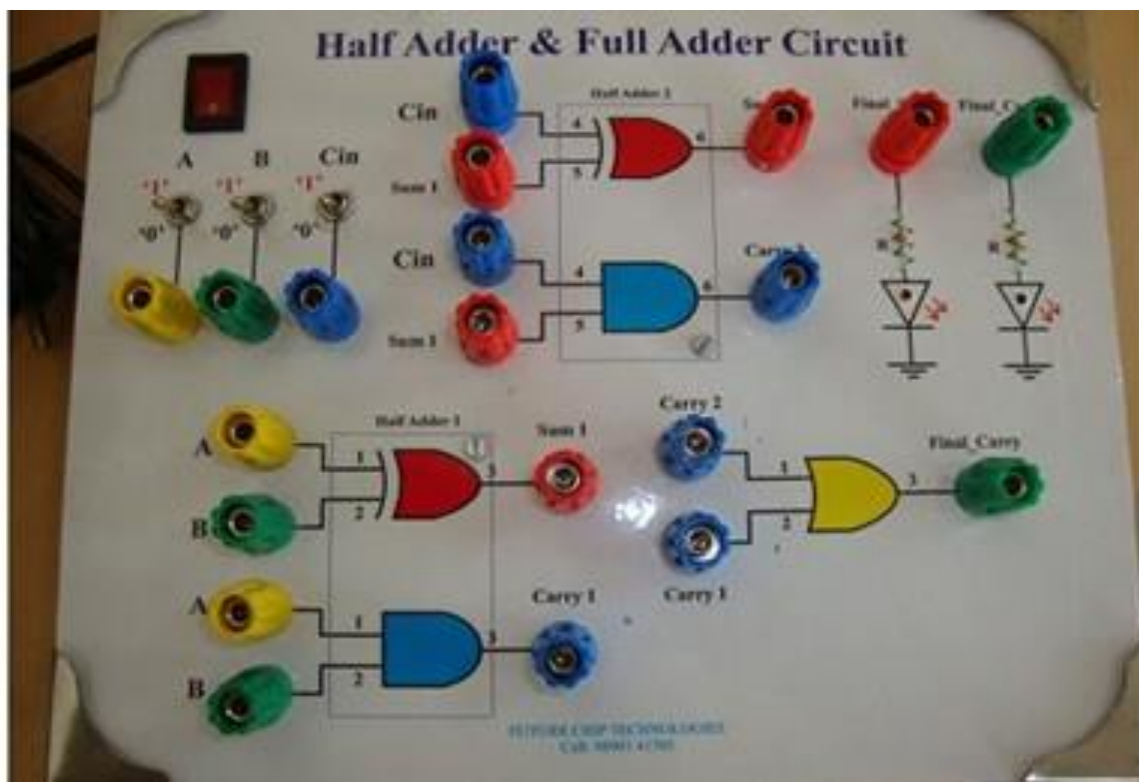
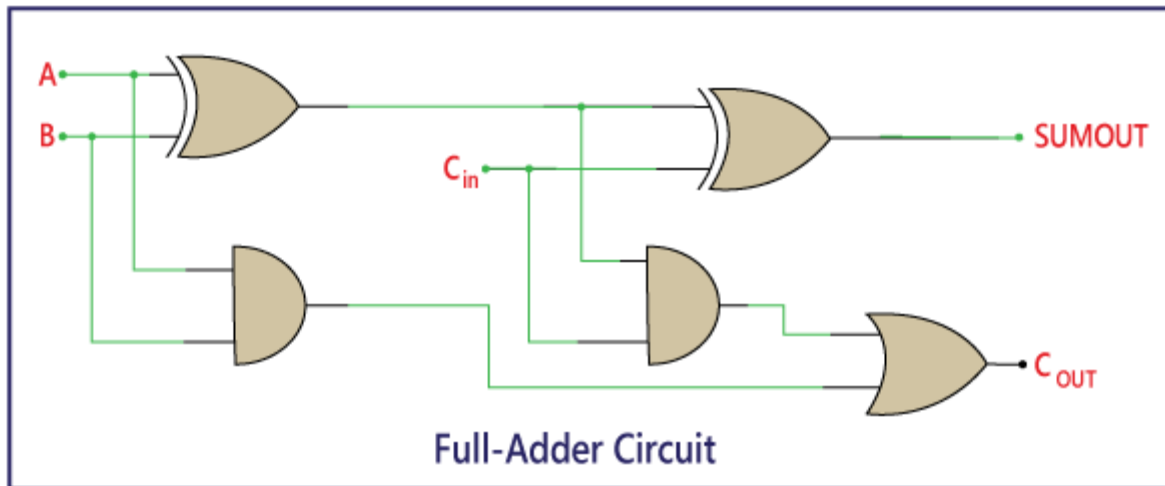
HALF ADDER



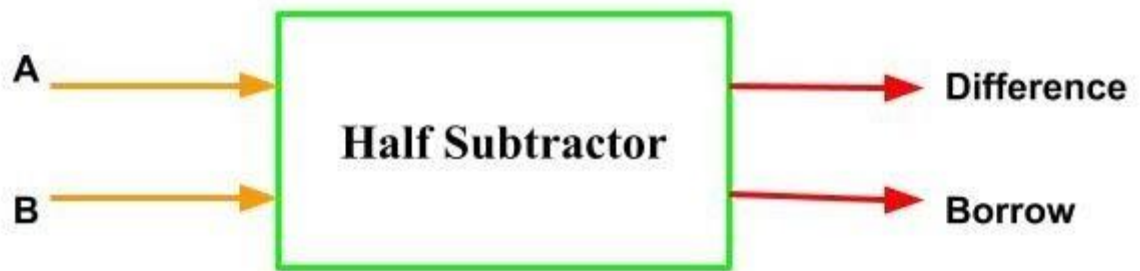
Truth Table			
Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



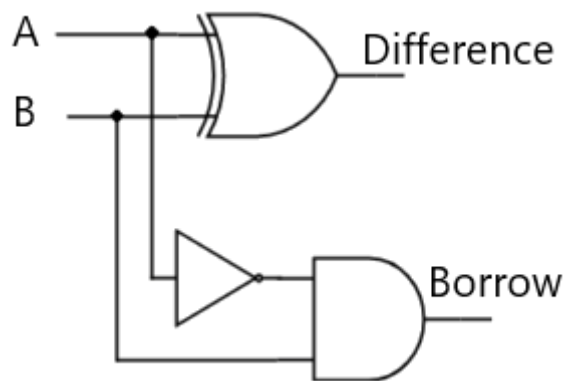
Inputs			Outputs	
A	B	C _{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



HALF SUBTRACTOR



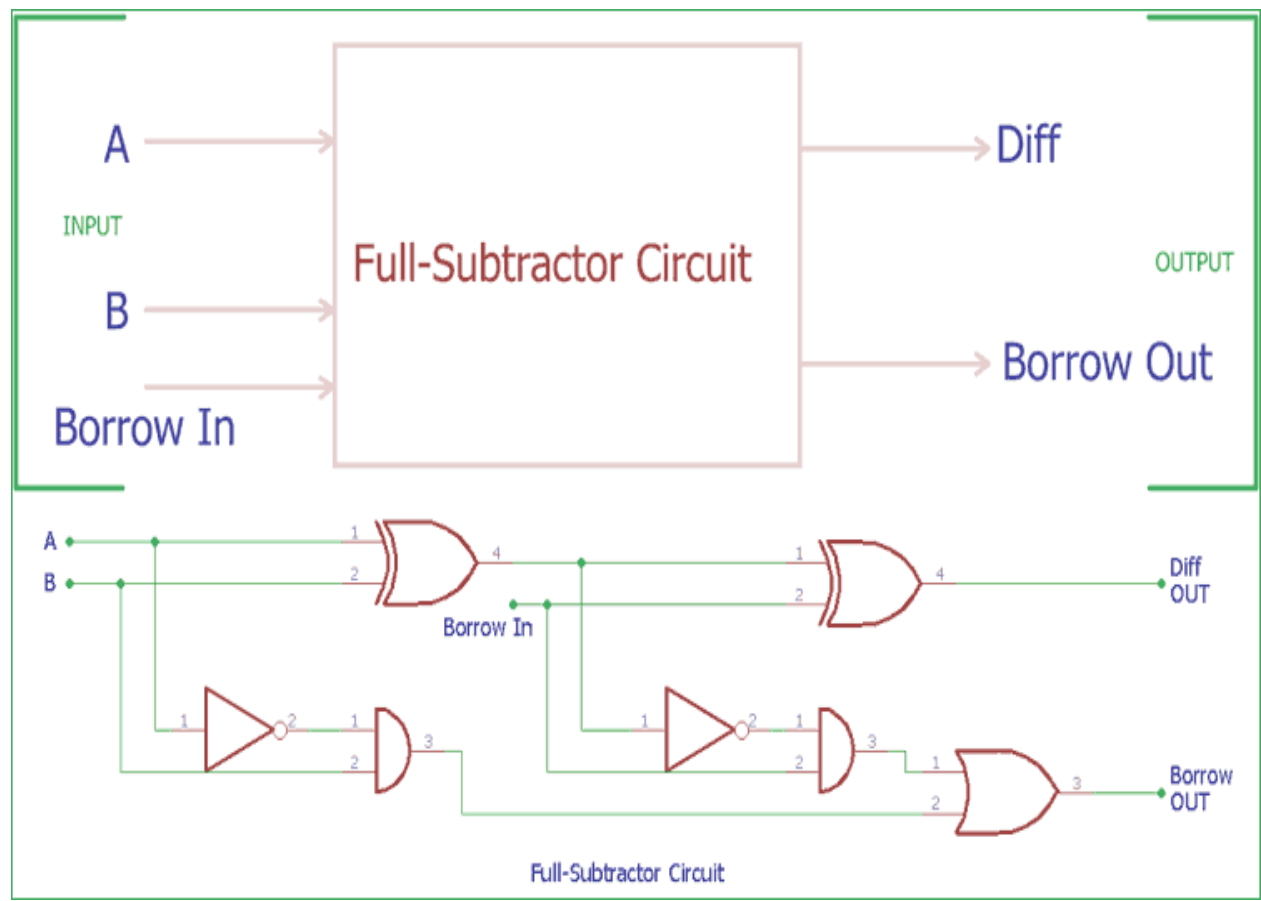
Inputs		Outputs	
A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0



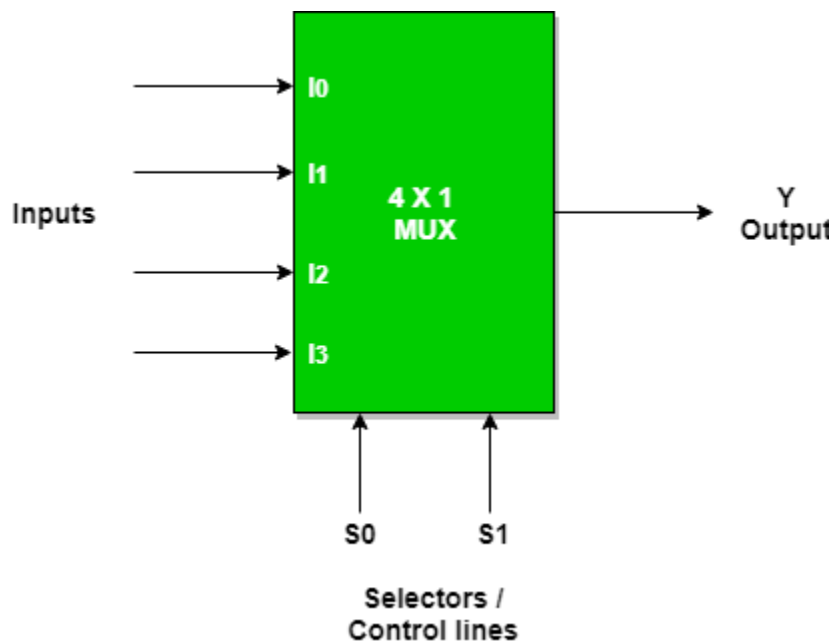
FULL SUBTRACTOR

Full Subtractor-Truth Table				
Input			Output	
A	B	C	Difference	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

www.flintgroups.com

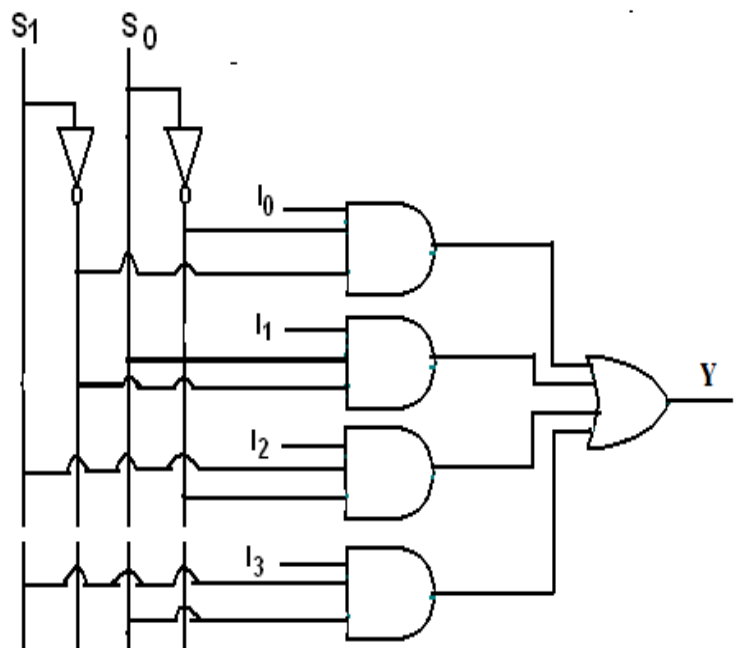


4:1 MULTIPLEXER



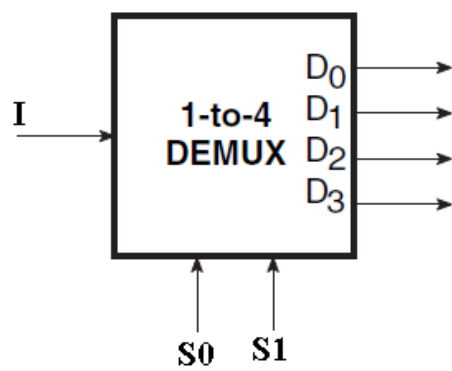
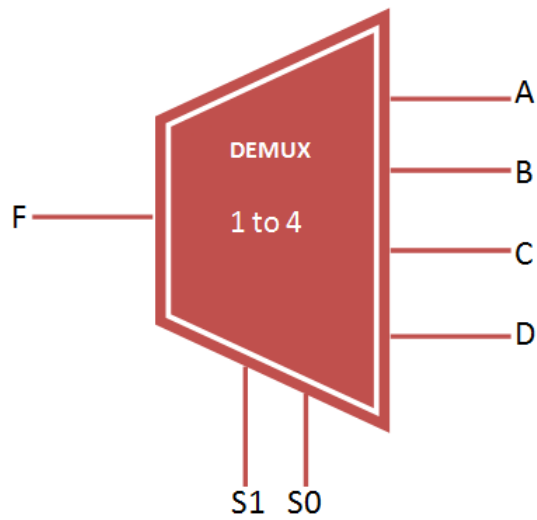
Input	S_1	S_0	Y
I_0	0	0	I_0
I_1	0	1	I_1
I_2	1	0	I_2
I_3	1	1	I_3

$$Y = S_1 S_0 I_3 + S_1 \bar{S}_0 I_2 + \bar{S}_1 S_0 I_1 + \bar{S}_1 \bar{S}_0 I_0$$

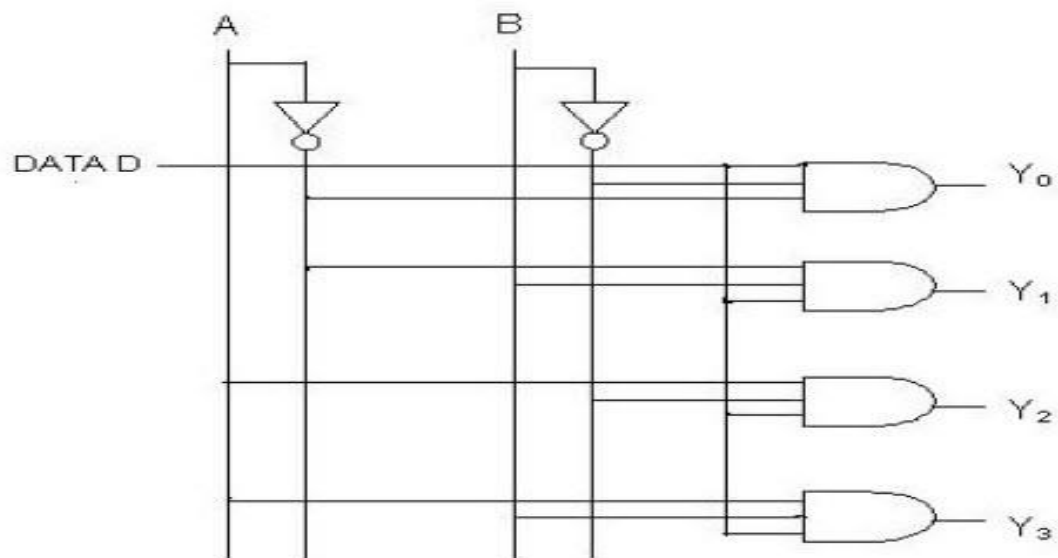


4 to 1 Multiplexer and its truth table

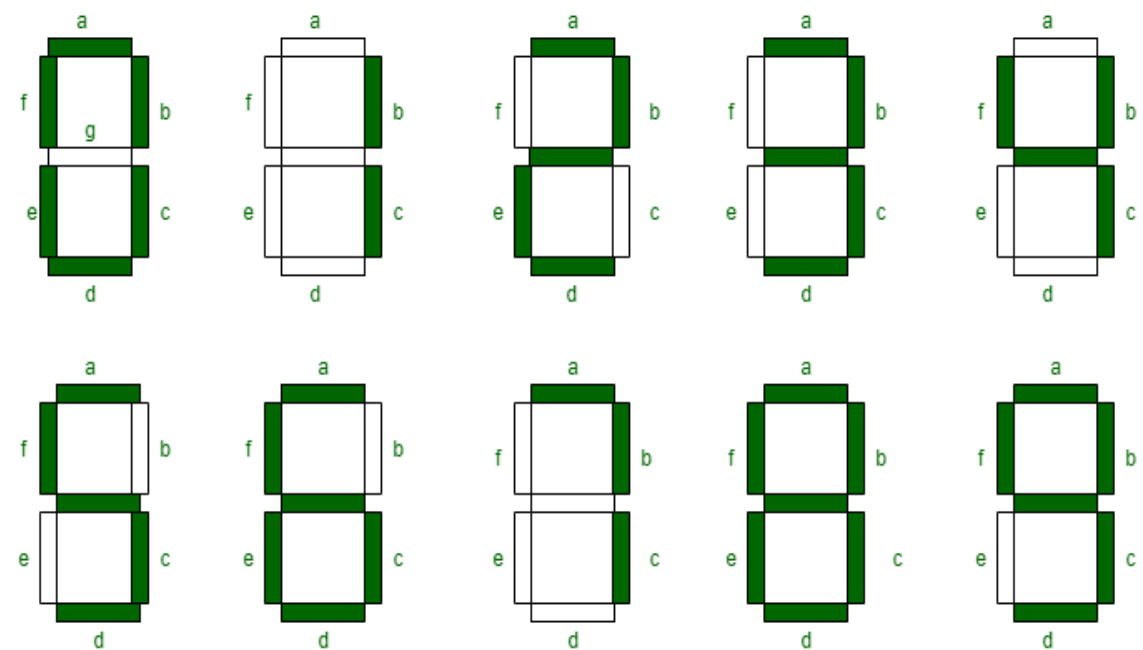
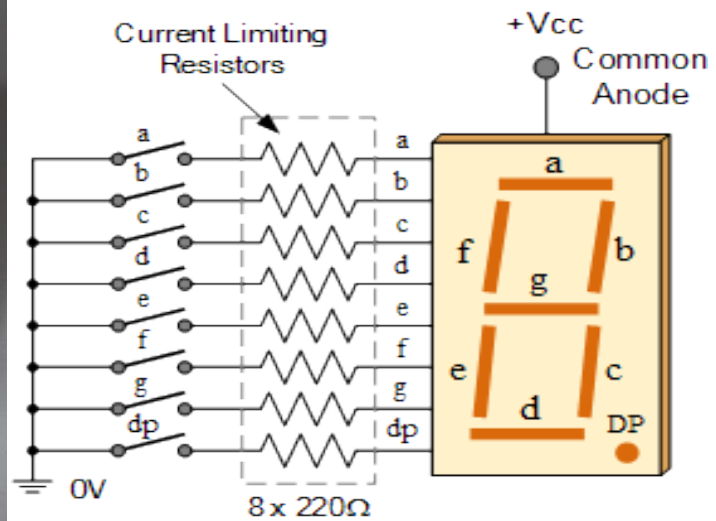
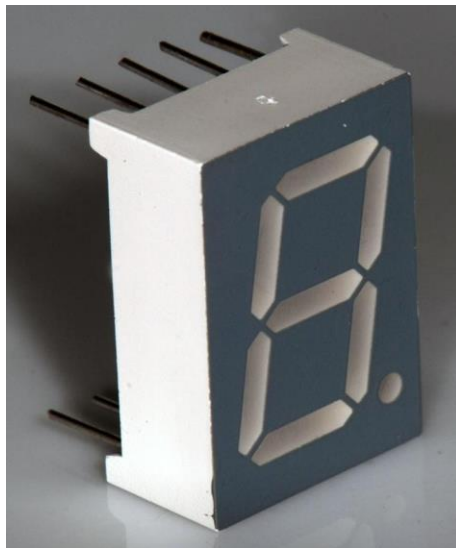
1:4 DEMULTIPLEXER



I	Select		O/P			
	S0	S1	D0	D1	D2	D3
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

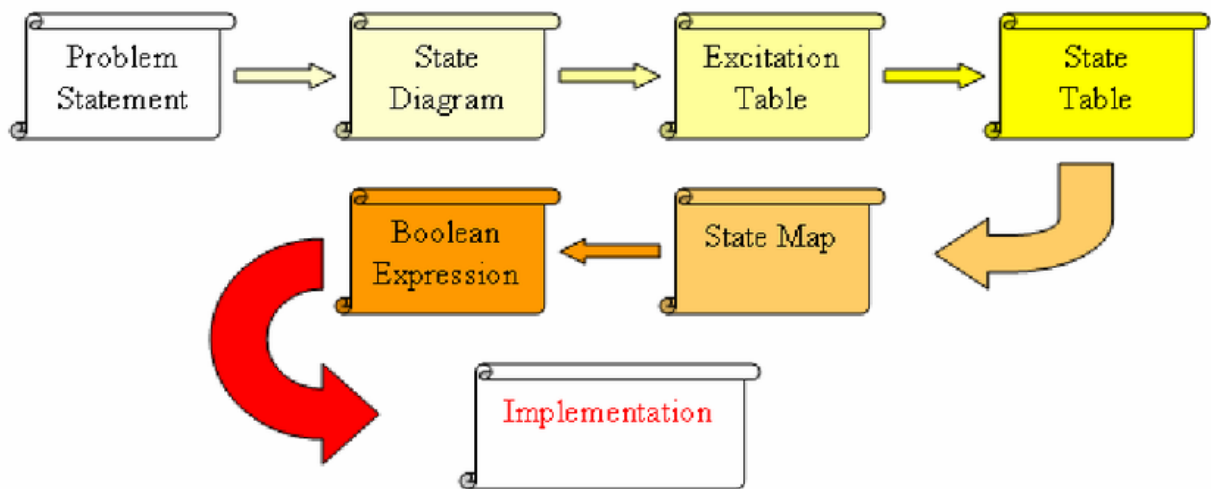


7 SEGMENT DISPLAY

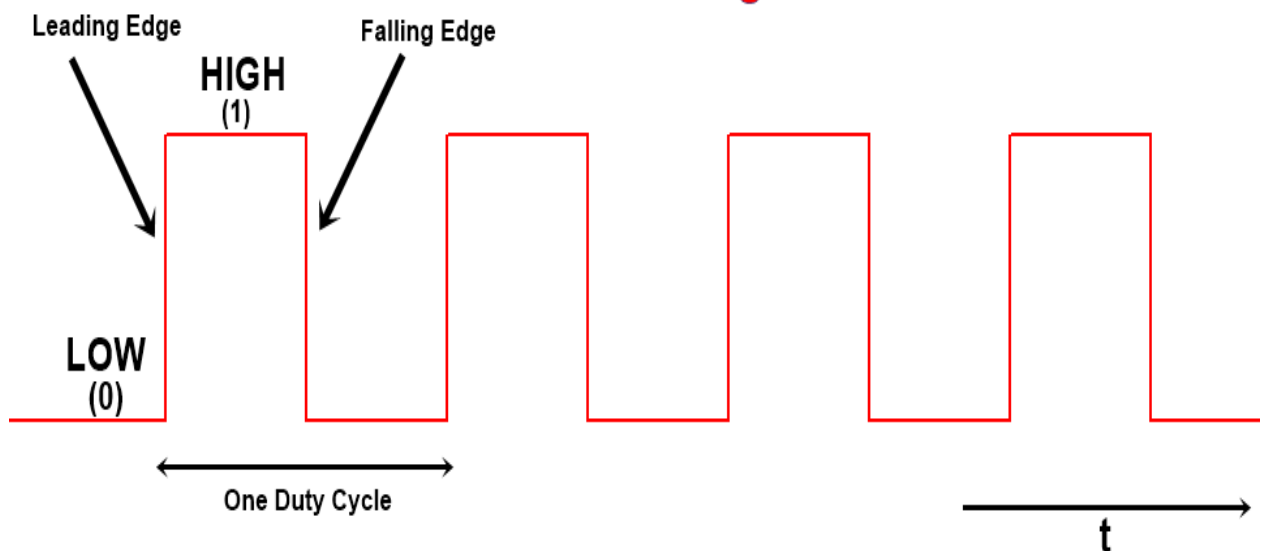


UNIT-3

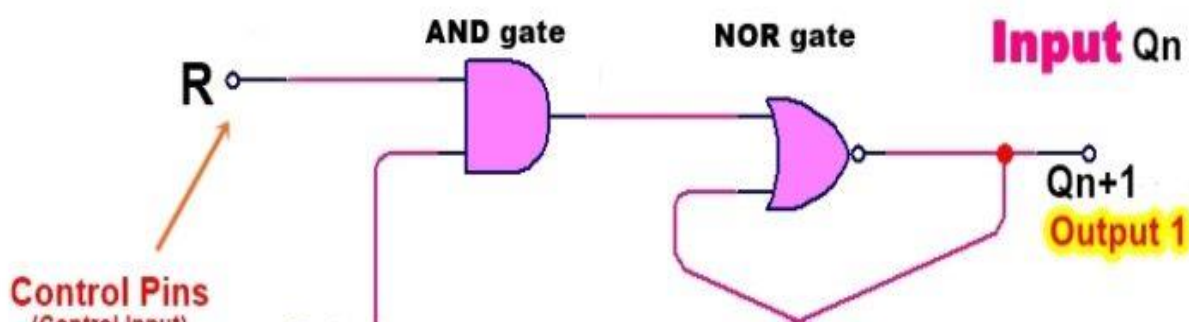
SEQUENTIAL CIRCUIT



Clock Signal/Pulse



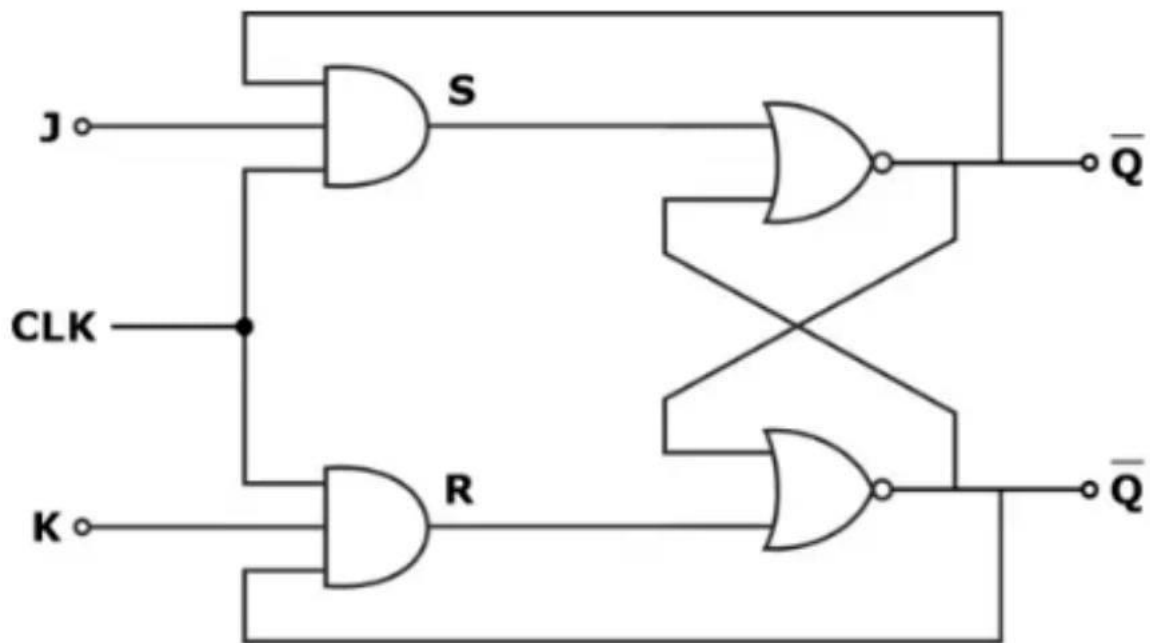
SR Flip-Flop



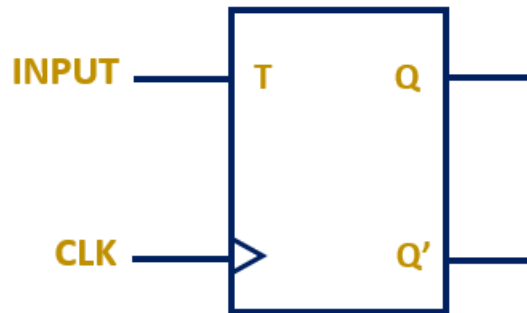
State	S	R	Q	Q'	Description
Set	1	0	0	1	Set Q'>>1
	1	1	0	1	No change
Reset	0	1	1	0	Reset Q'>>0
	1	1	1	0	No change
Invalid	0	0	1	1	Invalid Condition

JK Flip-Flop

$$S = J\bar{Q} \quad \text{and} \quad R = KQ$$

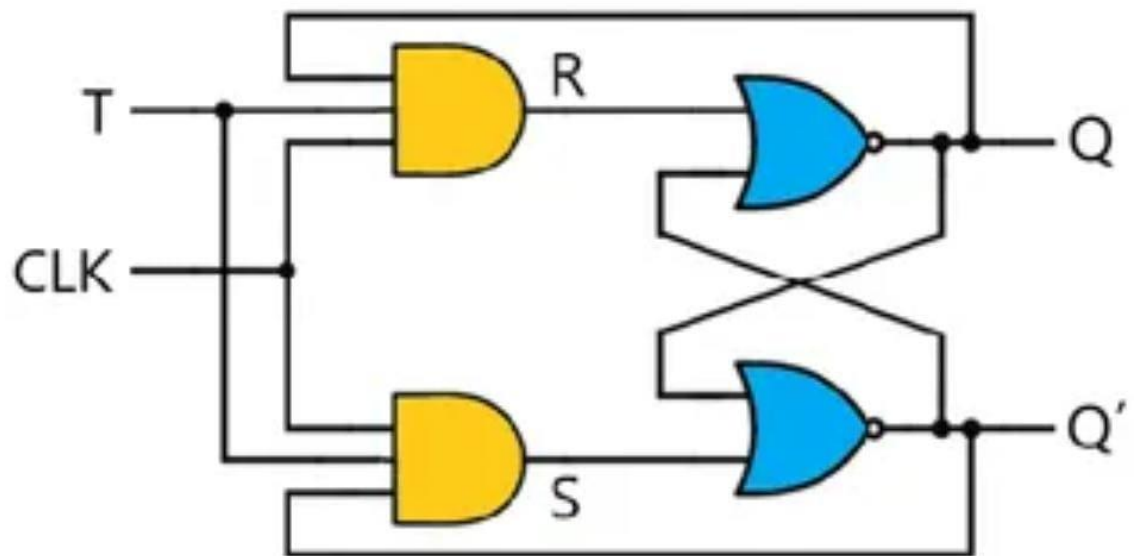


T Flip-Flop

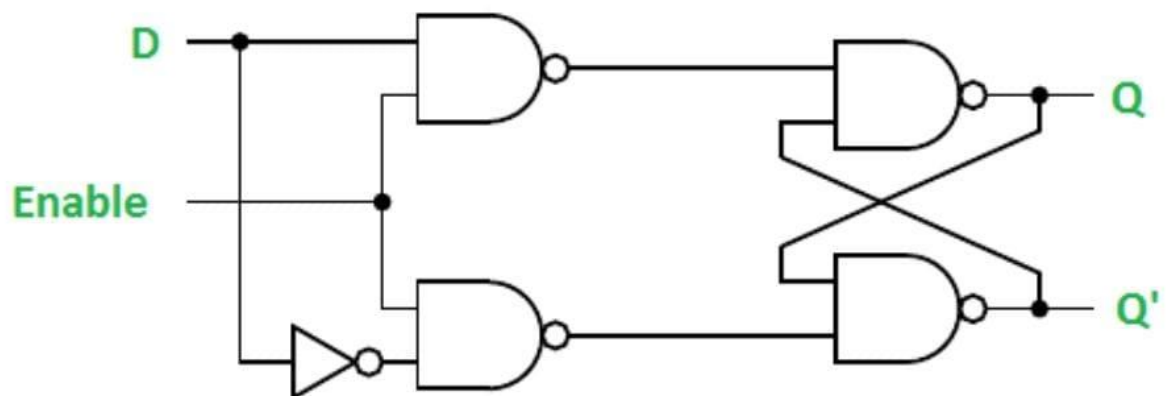


Clock	J	K	Q_{n+1}	State
0	X	X	Q_n	
1	0	0	Q_n	Hold
1	0	1	0	Reset
1	1	1	1	Set
1	1	1	$\overline{Q_n}$	Toggle

T FLIP-FLOP



D FLIP-FLOP



Truth Table for the D-type Flip Flop

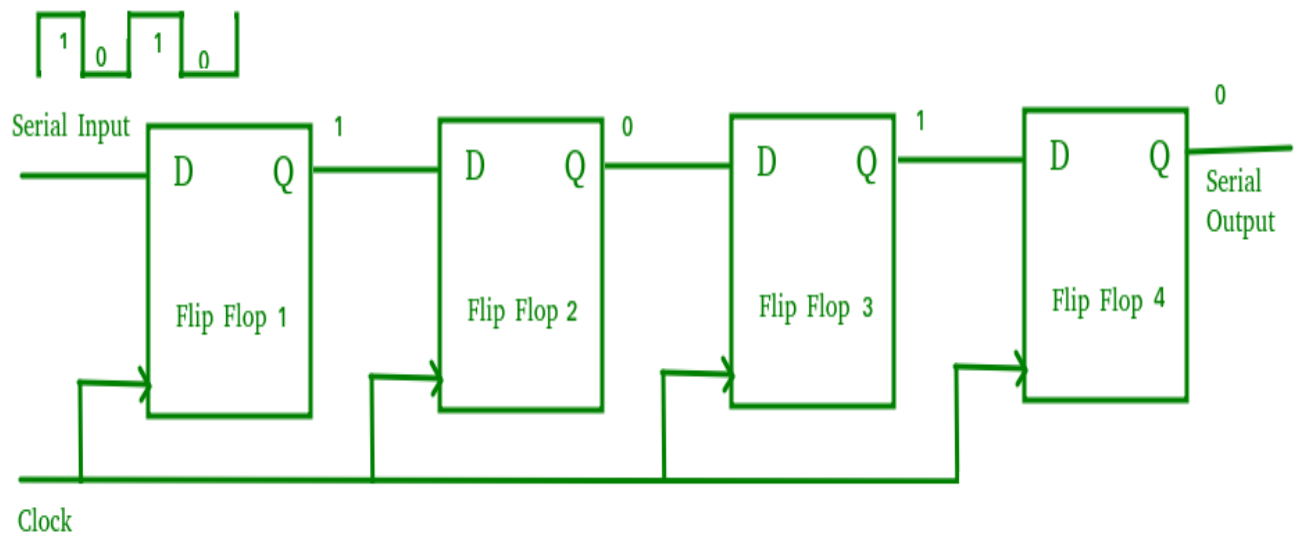
Clock	D	Q	Q'	Description
↓ » 0	X	Q	Q'	Memory no change
↑ » 1	0	0	1	Reset Q » 0
↑ » 1	1	1	0	Set Q » 1

Symbols ↓ and ↑ indicates the direction of the clock pulse. D-type flip flop assumed these symbols as edge-triggers.

UNIT-4:

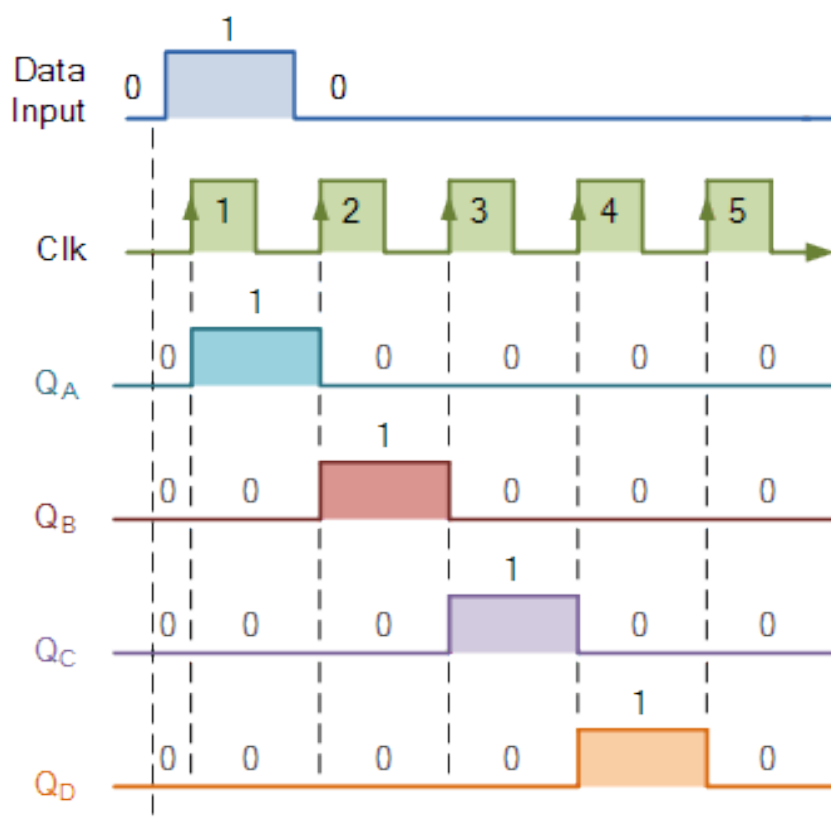
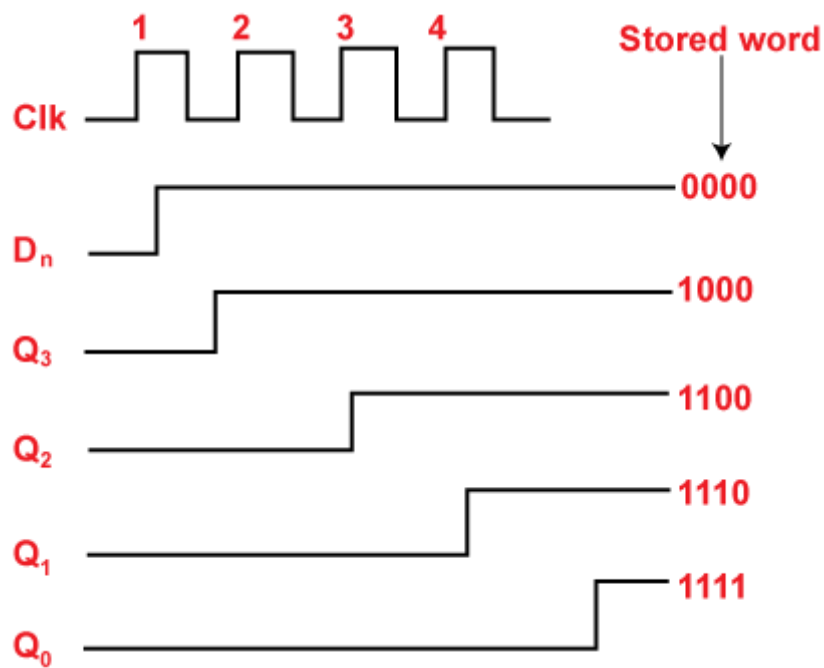
REGISTERS, MEMORIES & PLD

SERIAL IN SERIAL OUT

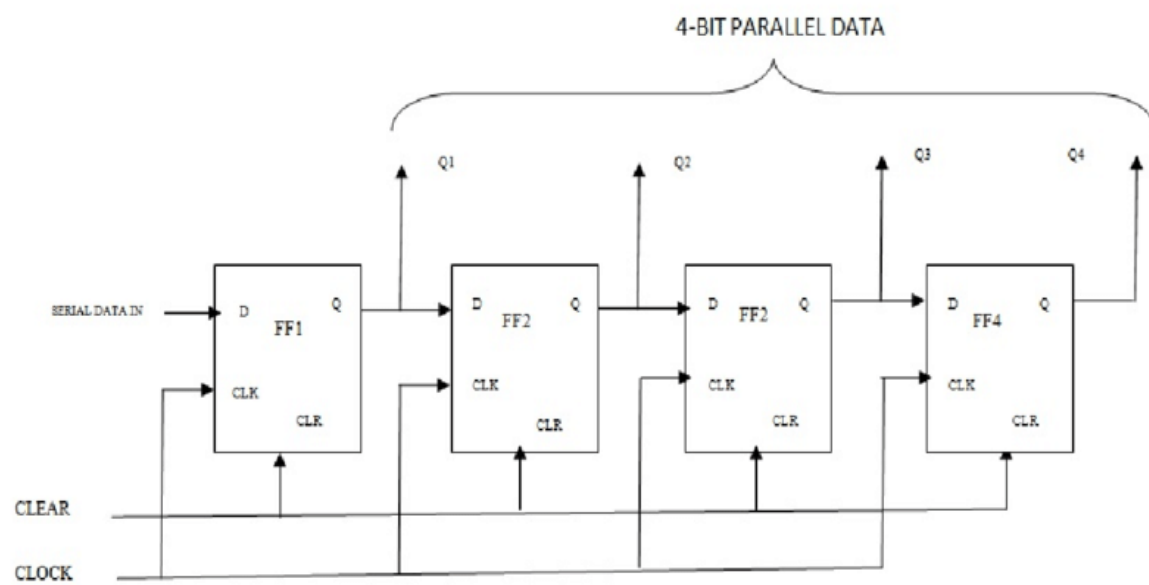


	Clk	$D_n = Q_3$	$Q_3 = D_2$	$Q_2 = D_1$	$Q_1 = D_0$	Q_0
Initially			0	0	0	0
(1)	↓	1 →	1	0	0	0
(2)	↓	1 →	1	1	0	0
(3)	↓	1 →	1	1	1	0
(4)	↓	1 →	1	1	1	1

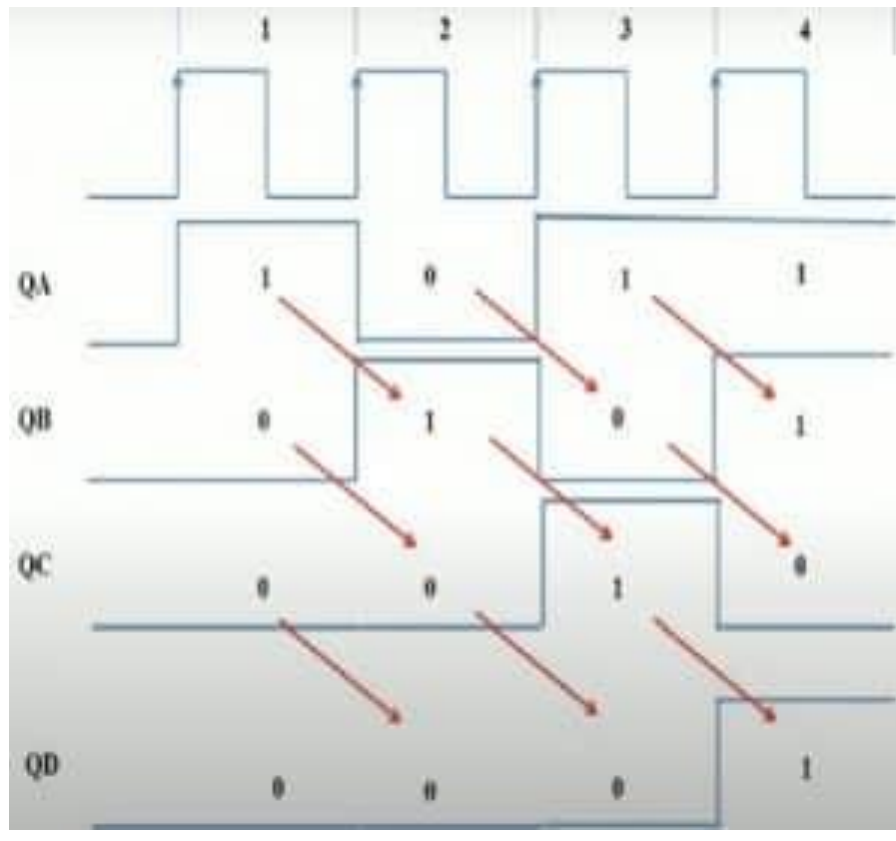
→ Direction of data travel



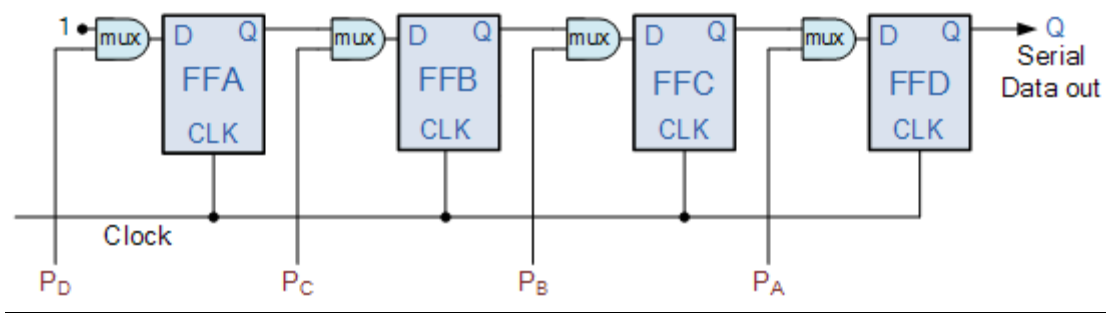
SERIAL- IN PARALLEL-OUT

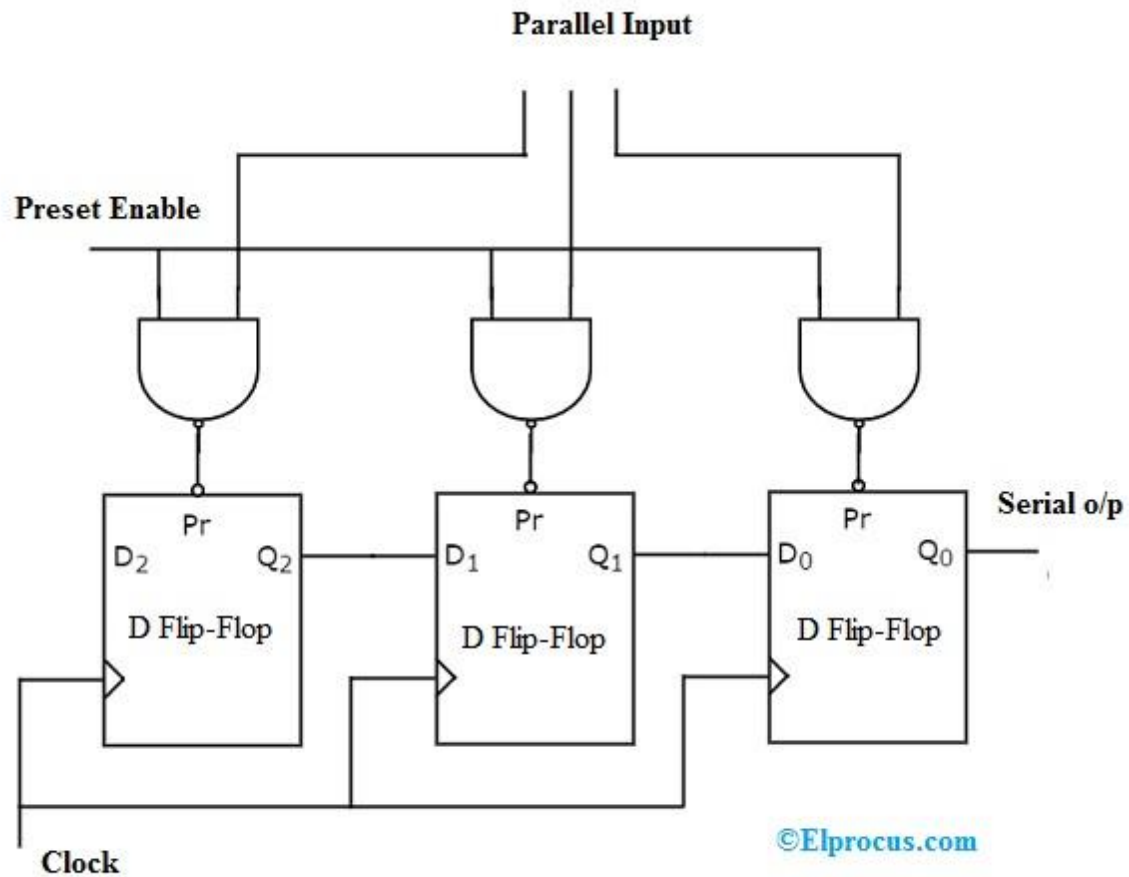


CLK Pulse	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	0	1	0
4	1	1	0	1



PARALLEL IN SERIAL OUT





PARALLEL IN PARALLEL OUT

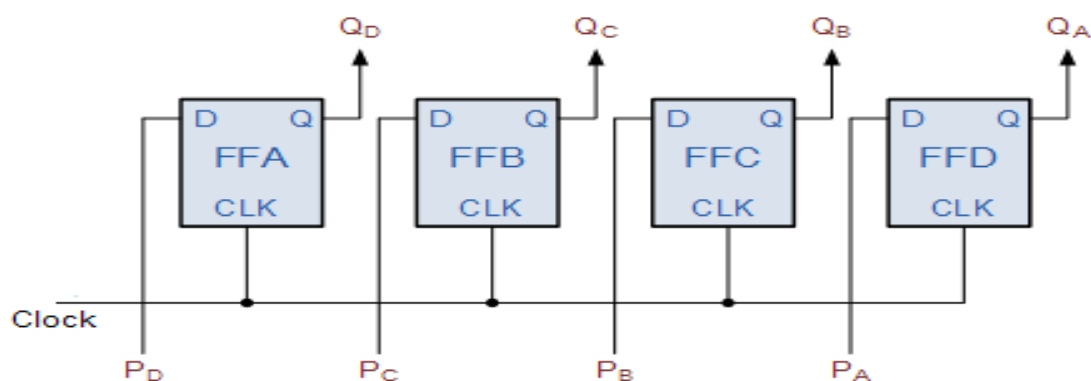


Table I Data Movement in Right-Shift PIPO Shift Register

Clock Cycle	SH / $\overline{\text{LD}}$	Q_1	Q_2	Q_3	...	Q_{n-1}	Q_n	
1	0	B_1	B_2	B_3		B_{n-1}	B_n	Parallel Data Loading ...
2	1	0	B_1	B_2	...	B_{n-2}	B_{n-1}	
3	1	0	0	B_1	...	B_{n-3}	B_{n-2}	
.		
.		
.		

Parallel Data Retrieval

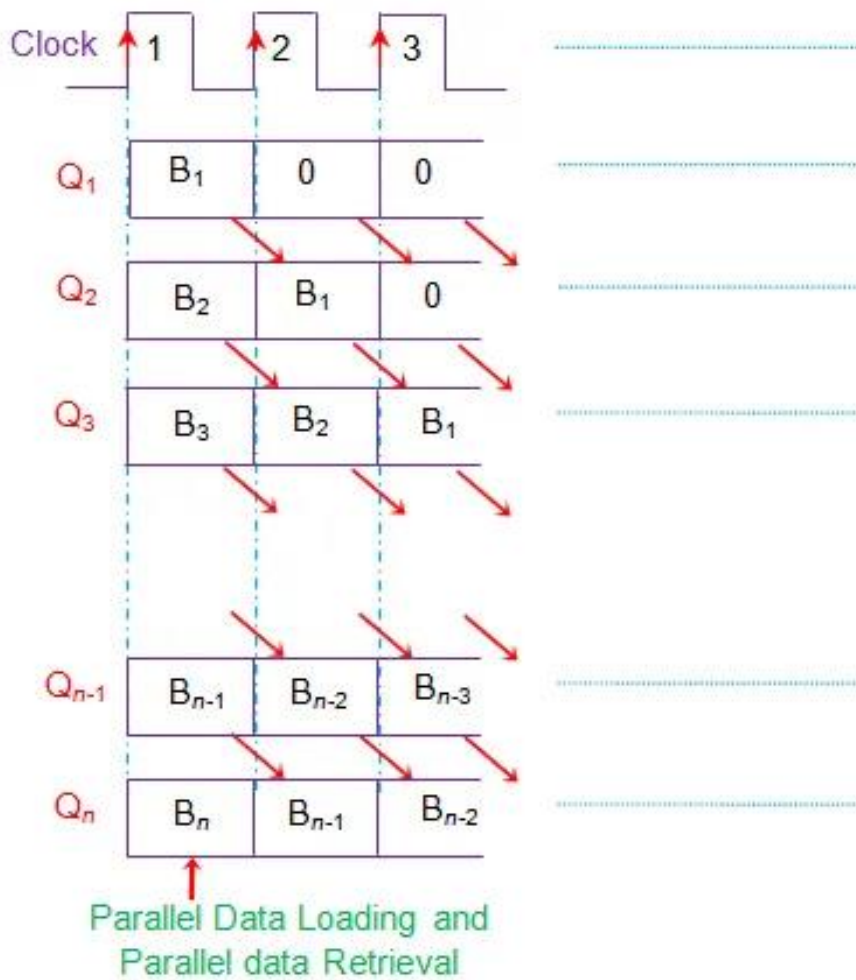
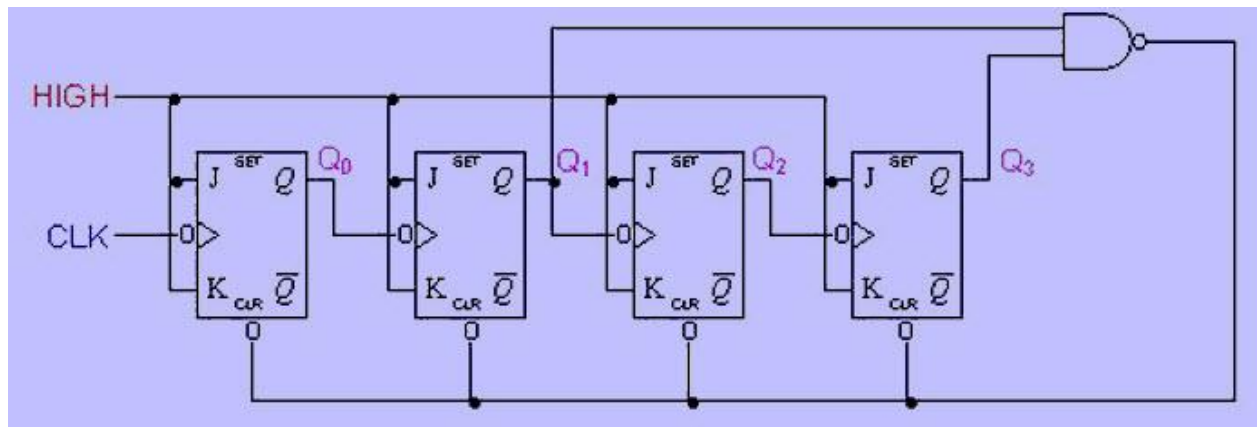


Figure 3 Output Waveform of n -bit Right-Shift PIPO Shift Register

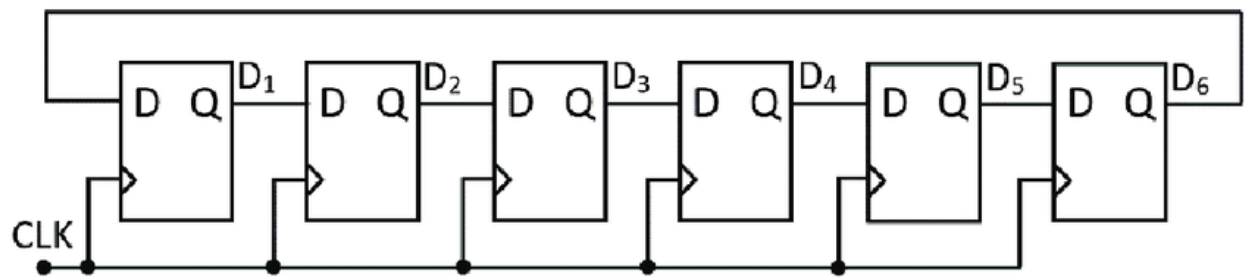
DECADE COUNTER



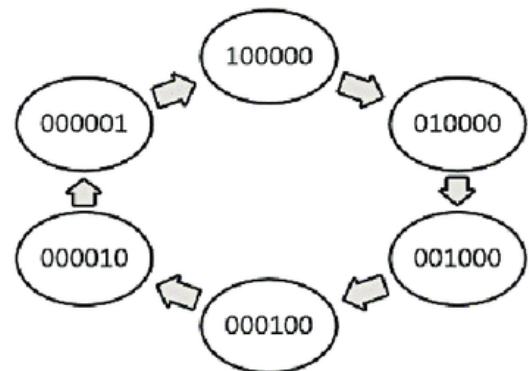
TRUTH TABLE

Clock Pulse	Q ₃	Q ₂	Q ₁	Q ₀
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

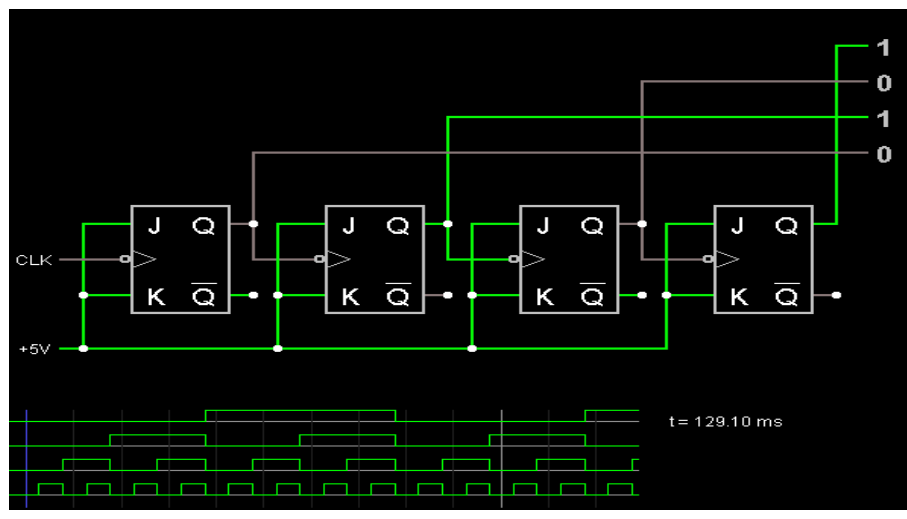
RING COUNTER



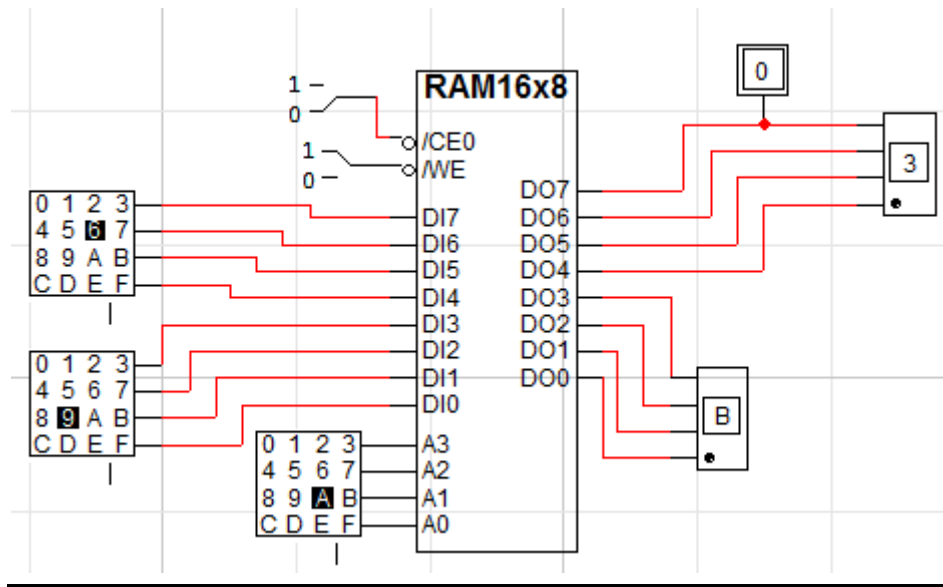
CLK	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆
1	1	0	0	0	0	0
2	0	1	0	0	0	0
3	0	0	1	0	0	0
4	0	0	0	1	0	0
5	0	0	0	0	1	0
6	0	0	0	0	0	1



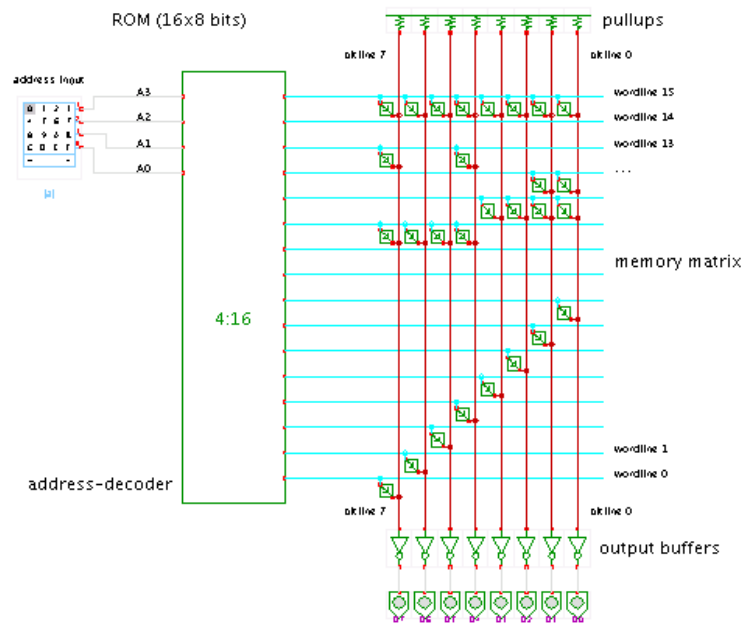
RIPPLE COUNTER



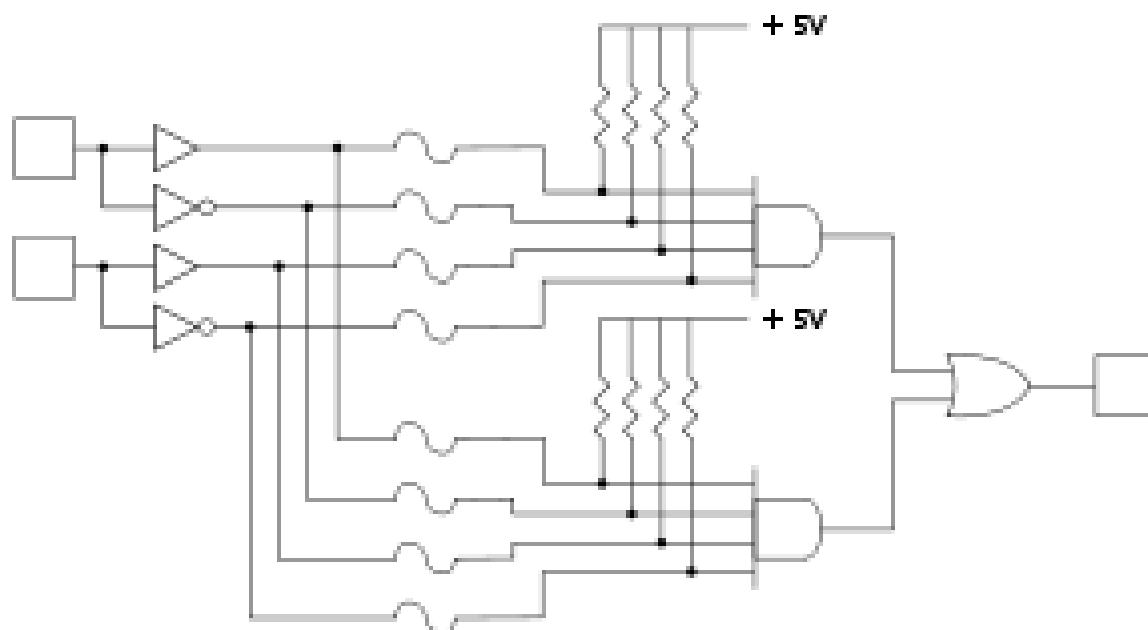
RAM



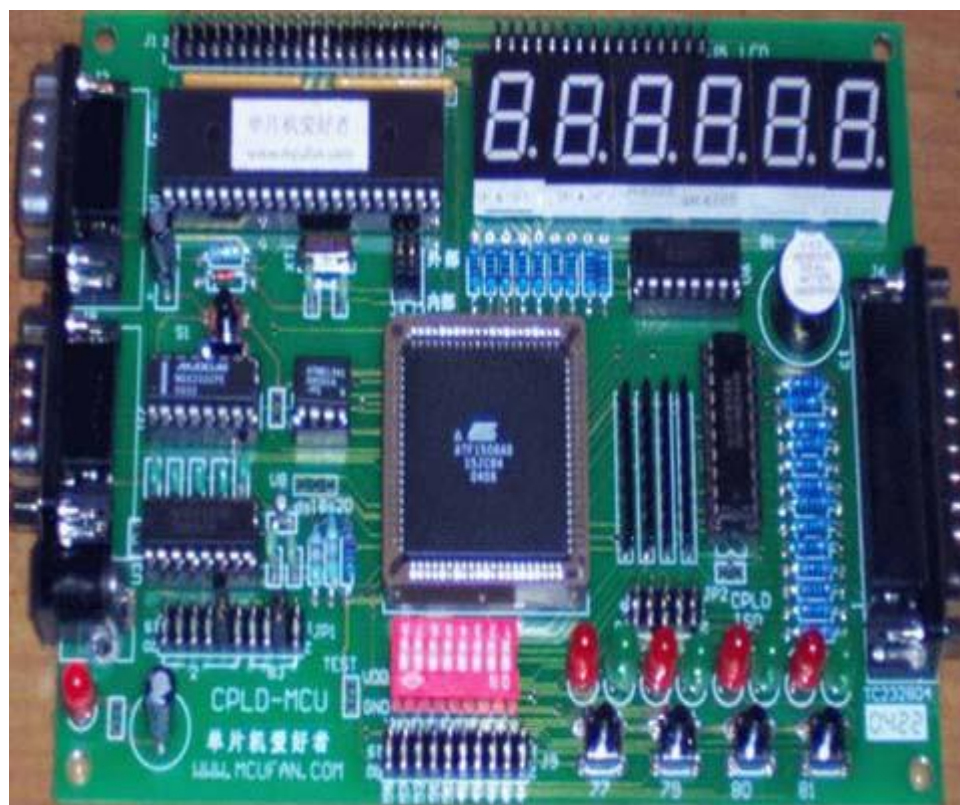
ROM



PLD

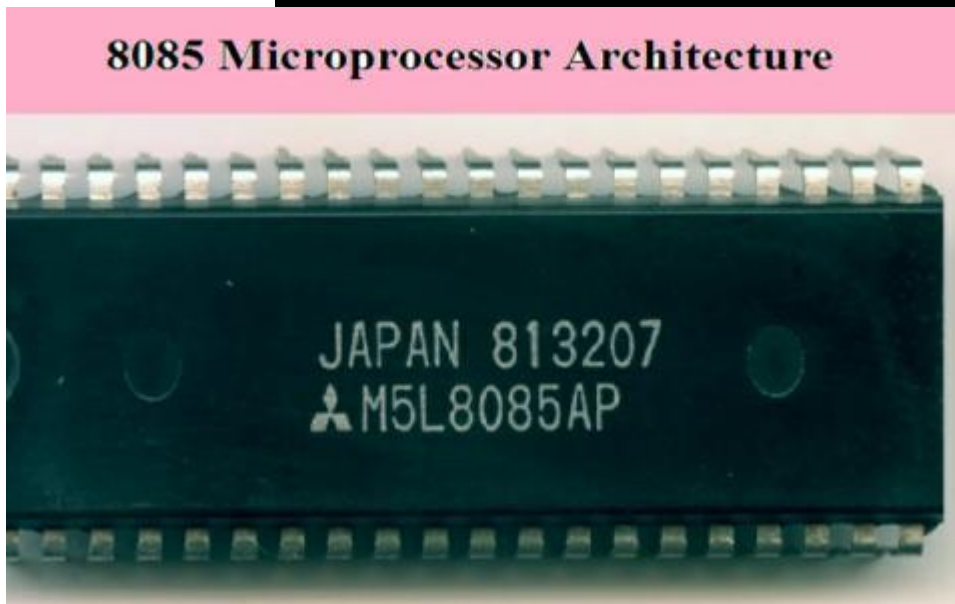


Simplified programmable logic device

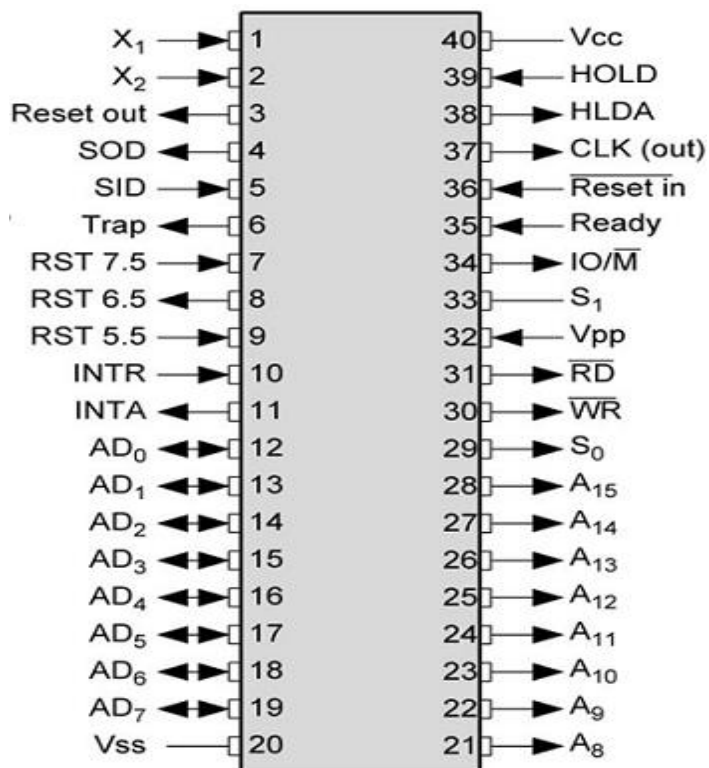


UNIT-4:

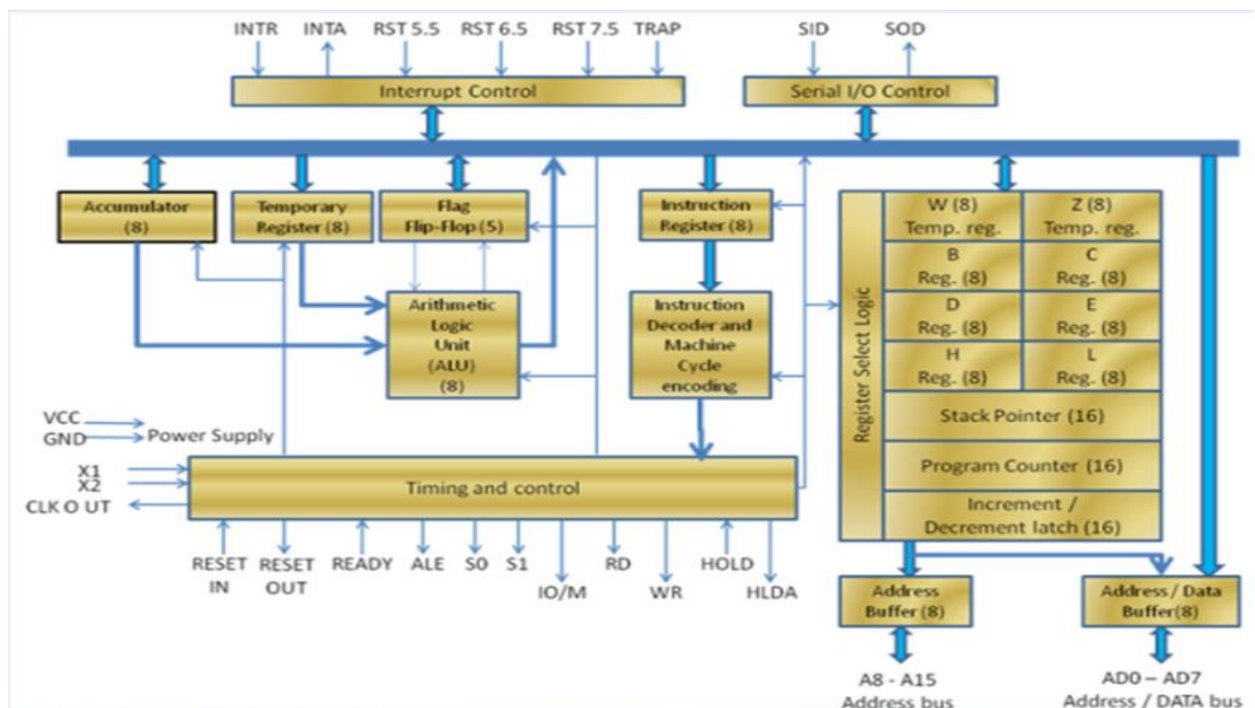
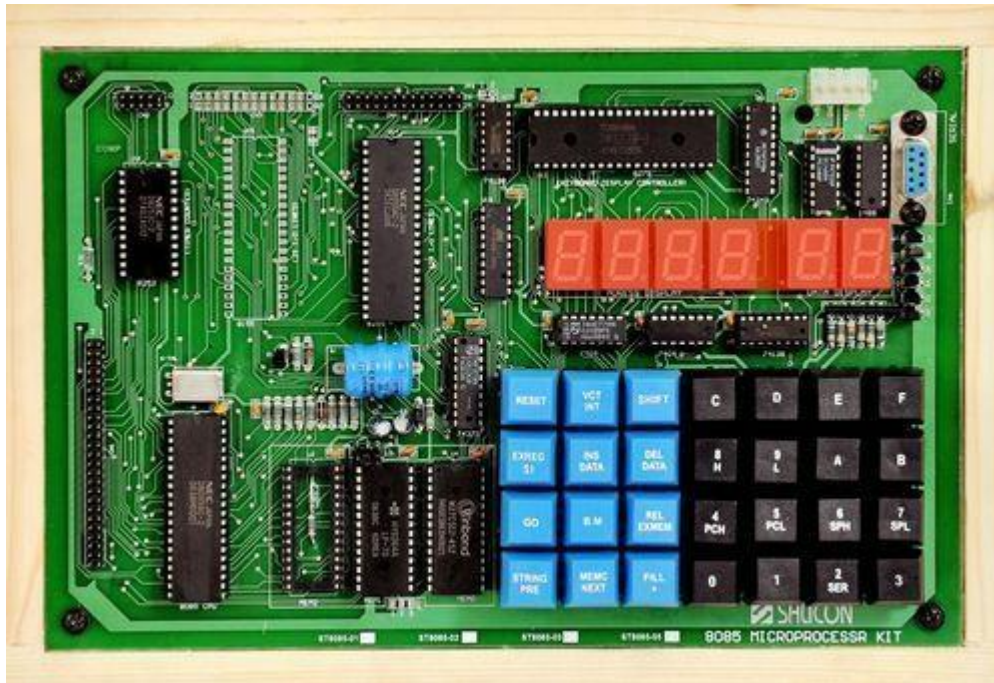
8085 MICROPROCESSOR



PIN DIAGRAM



ARCHITECTURE OF INTEL 8085A MICROPROCESSOR



UNIT-5:
INTERFACING AND SUPPORT CHIPS
Intel 8255



FUNCTIONAL BLOCK DIAGRAM

