



GANDHI SCHOOL OF ENGINEERING

BHABANDHA, BERHAMPUR

SESSION PLAN

3RD SEMESTER, BRANCH-INFORMATION TECHNOLOGY

COMPUTER SYSTEM ARCHITECTURE (TH-1)

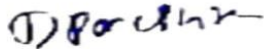
Name of the Faculty –ER. SANTOSH KUMAR BISHOYEE

Topics to be taken				TOPIC NO.	Actually Taken		
SL NO & CHAPTER	No. of Periods assigned by SCTE & VT	Details of the topics	PLANNING DATE		Details of the topics	ACTUAL DATE	Remarks
1 Basic structure of computer hardware	6	Basic structure of computer hardware: 1.1 Basic Structure of computer hardware 1.2 Functional Units 1.3 Computer components 1.4 Performance measures 1.5 Memory addressing & Operations	03-07-2024 TO 20-07-2024	1	Basic structure of computer hardware:	03-07-2024	
				1.1	1.1 Basic Structure of computer hardware	06-07-2024	
				1.2	1.2 Functional Units	11-07-2024	
				1.3	1.3 Computer components	13-07-2024	
				1.4	1.4 Performance measures	18-07-2024	
				1.5	1.5 Memory addressing & Operations	20-07-2024	
2 Instructions & instruction Sequencing	7	Instructions & instruction Sequencing: 2.1 Fundamentals to instructions 2.2 Operands 2.3 Op Codes 2.4 Instruction formats 2.5 Addressing Modes	11-07-2024 TO 24-07-2024	2	Instructions & instruction Sequencing:	22-07-2024	
				2.1	2.1 Fundamentals to instructions	24-07-2024	
				2.2	2.2 Operands	27-07-2024	
				2.3	2.3 Op Codes	29-07-2024	
				2.4	2.4 Instruction formats	31-07-2024	
				2.5	2.5 Addressing Modes	01-08-2024 05-08-2024	
3 Processor System	10	Processor System: 3.1 Register Files 3.2 Complete instruction execution Fetch Decode Execution 3.3 Hardware control 3.4 Micro program control	30-07-2024 TO 14-08-2024	3	Processor System: INTRODUCTION	08-08-2024	
				3.1	3.1 Register Files	10-08-2024	
					Register Files	12-08-2024	
					3.2 Complete instruction execution	14-08-2024	
				3.2	Fetch	17-08-2024	
					Decode	21-08-2024	
					Execution	22-08-2024	
					Fetch, Decode, Execution	29-08-2024	
				3.3	3.3 Hardware control	31-08-2024	
				3.4	3.4 Micro program control	09-04-2024	

4 Memory System	10	Memory System:	09-09-2024 TO 03-10-2024	4	Memory System: INTRODUCTION	09-09-2024	
		4.1Memory characteristics		4.1	4.1Memory characteristics	09-11-2024	
		4.2 Memory hierarchy		4.2	Memory characteristics	14-09-2024	
		4.3 RAM and ROM organization		4.3	4.2 Memory hierarchy	18-09-2024	
		4.4 Interleaved Memory		4.4	Memory hierarchy	19-09-2024	
		4.5 Cache memory		4.5	4.3 RAM and ROM organization	21-09-2024	
		4.6 Virtual memory		4.6	4.4 Interleaved Memory	23-09-2024	
5 Input – Output System	10	Input – Output System:	05-10-2024 TO 11-11-2024	5	Input – Output System: INTRODUCTION	05-10-2024	
		5.1 Input - Output Interface		5.1	Input – Output System: INTRODUCTION	21-10-2024	
		5.2 Modes of Data transfer		5.2	5.1 Input - Output Interface	26-10-2024	
		5.3 Programmed I/O Transfer		5.3	5.2 Modes of Data transfer	30-10-2024	
		5.4 Interrupt driven I/O		5.4	5.3 Programmed I/O Transfer	02-11-2024	
		5.5 DMA		5.5	Programmed I/O Transfer	04-11-2024	
		5.6 I/O Processor		5.6	5.4 Interrupt driven I/O	06-11-2024	
6 I/O Interface & Bus architecture	10	I/O Interface & Bus architecture:	16-11-2024 TO 04-12-2024	6	I/O Interface & Bus architecture:INTRODUCTION	16-11-2024	
		6.1 Bus and System Bus		6.1	6.1 Bus and System Bus	18-11-2024	
		6.2 Types of System Bus		6.2	6.2 Types of System Bus	20-11-2024	
		□ Data		6.2	□ Data	21-11-2024	
		□ Address		6.3	□ Address	25-11-2024	
		□ Control7.1 Bus		6.4	□ Control7.1 Bus	27-11-2024	
		6.3 Bus Structure		6.5	6.3 Bus Structure	28-11-2024	
		6.4 Basic Parameters of Bus design		6.6	6.4 Basic Parameters of Bus design	30-11-2024	
		6.5 SCSI		6.6	6.5 SCSI	02-12-2024	
		6.6 USB		6.6	6.6 USB	04-12-2024	

7 Parallel Processing	7	Parallel Processing:	05-12-2024 TO 16-12-2024	7	Parallel Processing: INTRODUCTION	05-12-2024	
		7.1 Parallel Processing		7.1	7.1 Parallel Processing	07-12-2024	
		7.2 Linear Pipeline		7.2	7.2 Linear Pipeline	09-12-2024	
		7.3 Multiprocessor		7.3	7.3 Multiprocessor	14-12-2024	
		7.4 Flynn"s Classification		7.4	7.4 Flynn"s Classification	06-12-2024	
					Flynn"s Classification	16-12-2024	

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