GANDHI SCHOOL OF ENGINEERING
BHABANDHA, BERHAMPUR
SESSION PLAN
3RD SEMESTER, BRANCH-INFORMATION TECHNOLOGY

COMPUTER SYSTEM ARCHITECTURE (TH-1)

Name of the Faculty –ER. SANTOSH KUMAR BISHOYEE

Topics to be taken				TOPIC NO.	Actually Taken		
SL NO & CHAPTER	No. of Periods assigned by SCTE & VT	Details of the topics	PLANNING DATE		Details of the topics	ACTUAL DATE	Remarks
1 Basic structure of computer hardware	6	**Basic structure of computer hardware:** 1.1Basic Structure of computer hardware 1.2Functional Units 1.3Computer components 1.4 Performance measures 1.5 Memory addressing & Operations	03-07-2024 TO 20-07-2024	1 1.1 1.2 1.3 1.4 1.5	**Basic structure of computer hardware:** 1.1Basic Structure of computer hardware 1.2Functional Units 1.3Computer components 1.4 Performance measures 1.5 Memory addressing & Operations	03-07-2024 06-07-2024 11-07-2024 13-07-2024 18-07-2024 20-07-2024	
2 Instructions & instruction Sequencing	7	**Instructions & instruction Sequencing:** 2.1 Fundamentals to instructions 2.2 Operands 2.3 Op Codes 2.4 Instruction formats 2.5 Addressing Modes	11-07-2024 TO 24-07-2024	2 2.1 2.2 2.3 2.4 2.5	**Instructions & instruction Sequencing:** 2.1 Fundamentals to instructions 2.2 Operands 2.3 Op Codes 2.4 Instruction formats 2.5 Addressing Modes	22-07-2024 24-07-2024 27-07-2024 29-07-2024 31-07-2024 01-08-2024 05-08-2024	
3 Processor System	10	**Processor System:** 3.1 Register Files 3.2 Complete instruction execution Fetch Decode Execution 3.3 Hardware control 3.4 Micro program control	30-07-2024 TO 14-08-2024	3 3.1 3.2 3.3 3.4	**Processor System: INTRODUCTION** 3.1 Register Files Register Files 3.2 Complete instruction execution Fetch Decode Execution Fetch, Decode, Execution 3.3 Hardware control 3.4 Micro program control	08-08-2024 10-08-2024 12-08-2024 14-08-2024 17-08-2024 21-08-2024 22-08-2024 29-08-2024 31-08-2024 09-04-2024	

4 Memory System	10	**Memory System:** 4.1Memory characteristics 4.2 Memory hierarchy 4.3 RAM and ROM organization 4.4 Interleaved Memory 4.5 Cache memory 4.6 Virtual memory	09-09-2024 TO 03-10-2024	4 4.1 4.2 4.3 4.4 4.5 4.6	**Memory System: INTRODUCTION** 4.1Memory characteristics Memory characteristics 4.2 Memory hierarchy Memory hierarchy 4.3 RAM and ROM organization 4.4 Interleaved Memory 4.5 Cache memory 4.6 Virtual memory Cache Memory & Virtual Memory	09-09-2024 09-11-2024 14-09-2024 18-09-2024 19-09-2024 21-09-2024 23-09-2024 25-09-2024 26-09-2024 10-03-2024	
5 Input – Output System	10	**Input – Output System:** 5.1 Input - Output Interface 5.2 Modes of Data transfer 5.3 Programmed I/O Transfer 5.4 Interrupt driven I/O 5.5 DMA 5.6 I/O Processor	05-10-2024 TO 11-11-2024	5 5.1 5.2 5.3 5.4 5.5 5.6	**Input – Output System: INTRODUCTION** Input – Output System: INTRODUCTION 5.1 Input - Output Interface 5.2 Modes of Data transfer 5.3 Programmed I/O Transfer Programmed I/O Transfer 5.4 Interrupt driven I/O 5.5 DMA 5.6 I/O Processor I/O Processor	05-10-2024 21-10-2024 26-10-2024 30-10-2024 02-11-2024 04-11-2024 06-11-2024 07-11-2024 09-11-2024 11-11-2024	
6 I/O Interface & Bus architecture	10	**I/O Interface & Bus architecture:** 6.1 Bus and System Bus 6.2 Types of System Bus ⍰ Data ⍰ Address ⍰ Control7.1 Bus 6.3 Bus Structure 6.4 Basic Parameters of Bus design 6.5 SCSI 6.6 USB	16-11-2024 TO 04-12-2024	6 6.1 6.2 6.3 6.4 6.5 6.6	**I/O Interface & Bus architecture:INTRODUCTION** 6.1 Bus and System Bus 6.2 Types of System Bus ⍰ Data ⍰ Address ⍰ Control7.1 Bus 6.3 Bus Structure 6.4 Basic Parameters of Bus design 6.5 SCSI 6.6 USB	16-11-2024 18-11-2024 20-11-2024 21-11-2024 25-11-2024 27-11-2024 28-11-2024 30-11-2024 02-12-2024 04-12-2024	

7 Parallel Processing	7	**Parallel Processing:** 7.1 Parallel Processing 7.2 Linear Pipeline 7.3 Multiprocessor 7.4 Flynn‟s Classification	05-12-2024 TO 16-12-2024	7 7.1 7.2 7.3 7.4	**Parallel Processing: INTRODUCTION** 7.1 Parallel Processing 7.2 Linear Pipeline 7.3 Multiprocessor 7.4 Flynn‟s Classification Flynn‟s Classification	05-12-2024 07-12-2024 09-12-2024 11-12-2024 14-12-2024 06-12-2024 16-12-2024	

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