GANDHI SCHOOL OF ENGINEERING,BHABANDHA,BERHAMPUR

TEACHING AND LEARNING MATERIAL

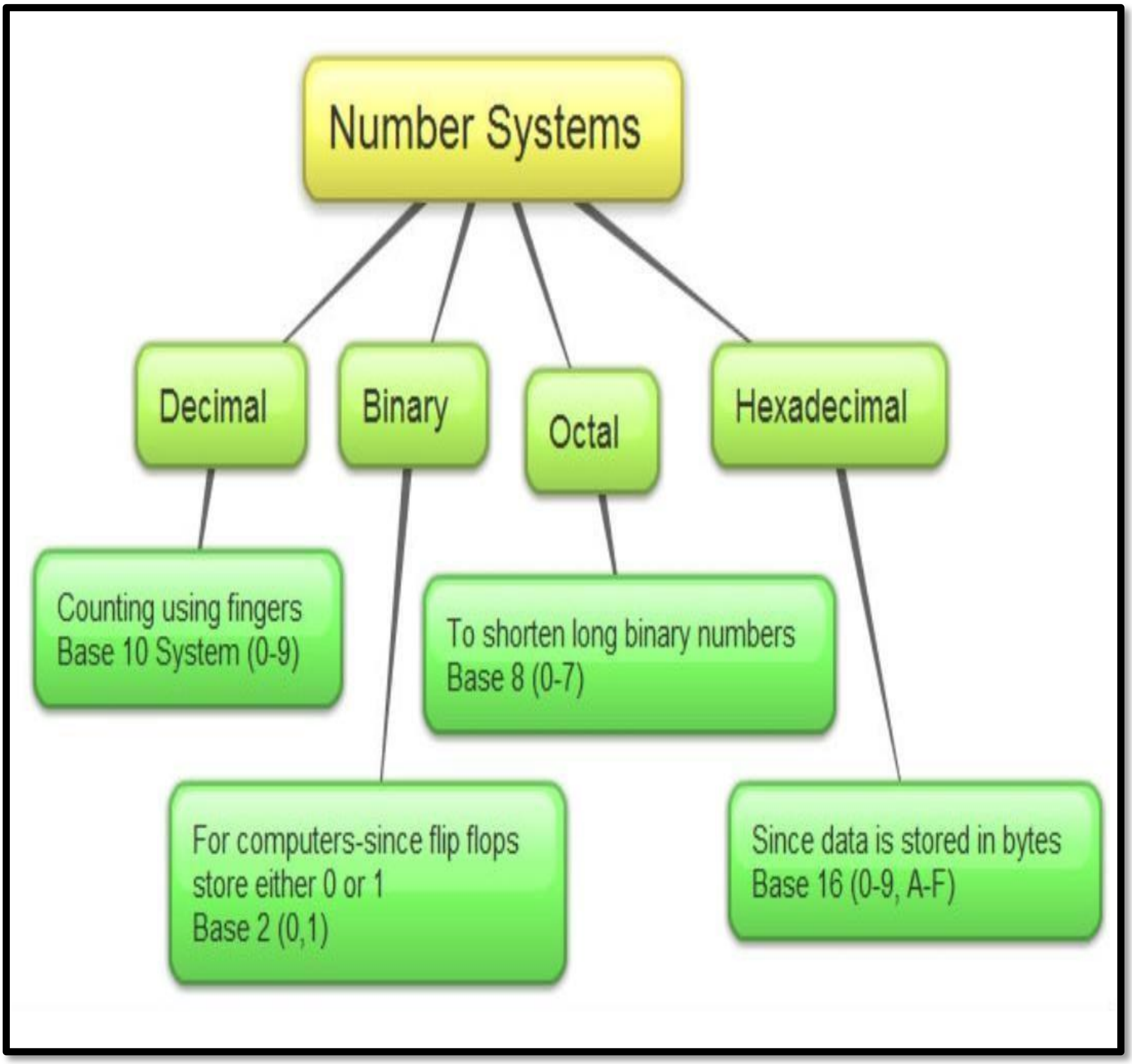
SUBJECT:DIGITAL ELECTRONICS

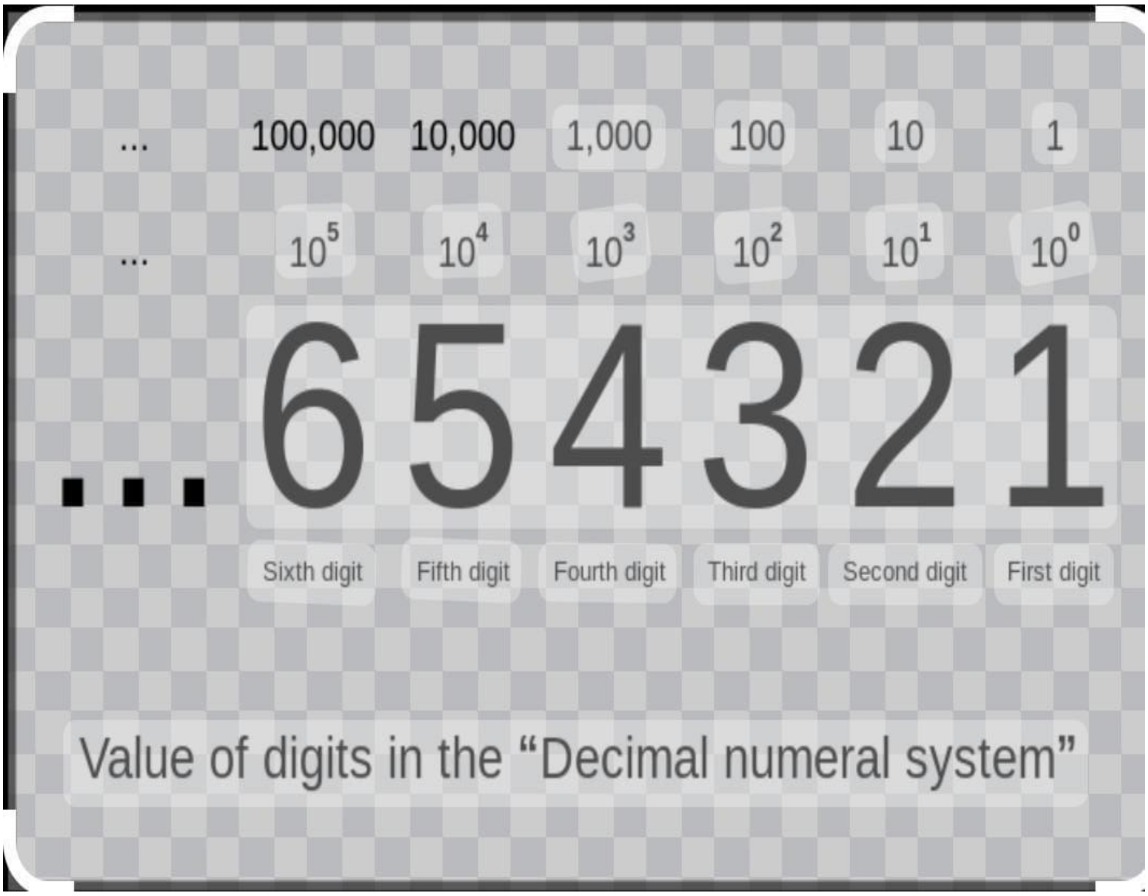
SEMESTER:3RD

SUBMITTED BY:-ER. SURABHI TRIPATHY

UNIT-1

NUMBER SYSTEM & CODES



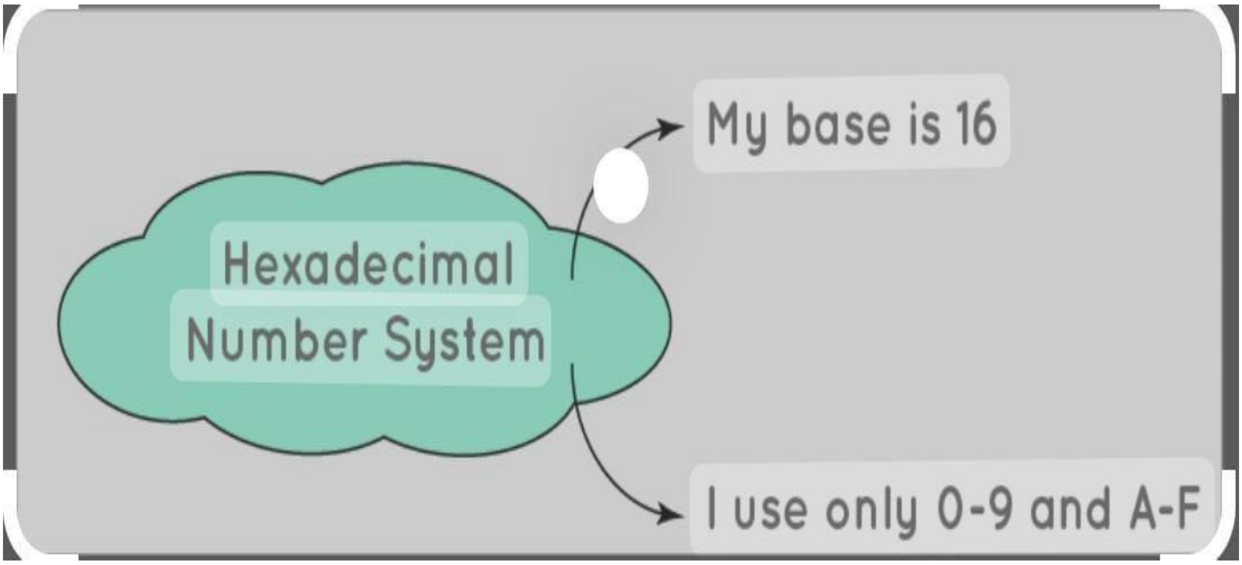


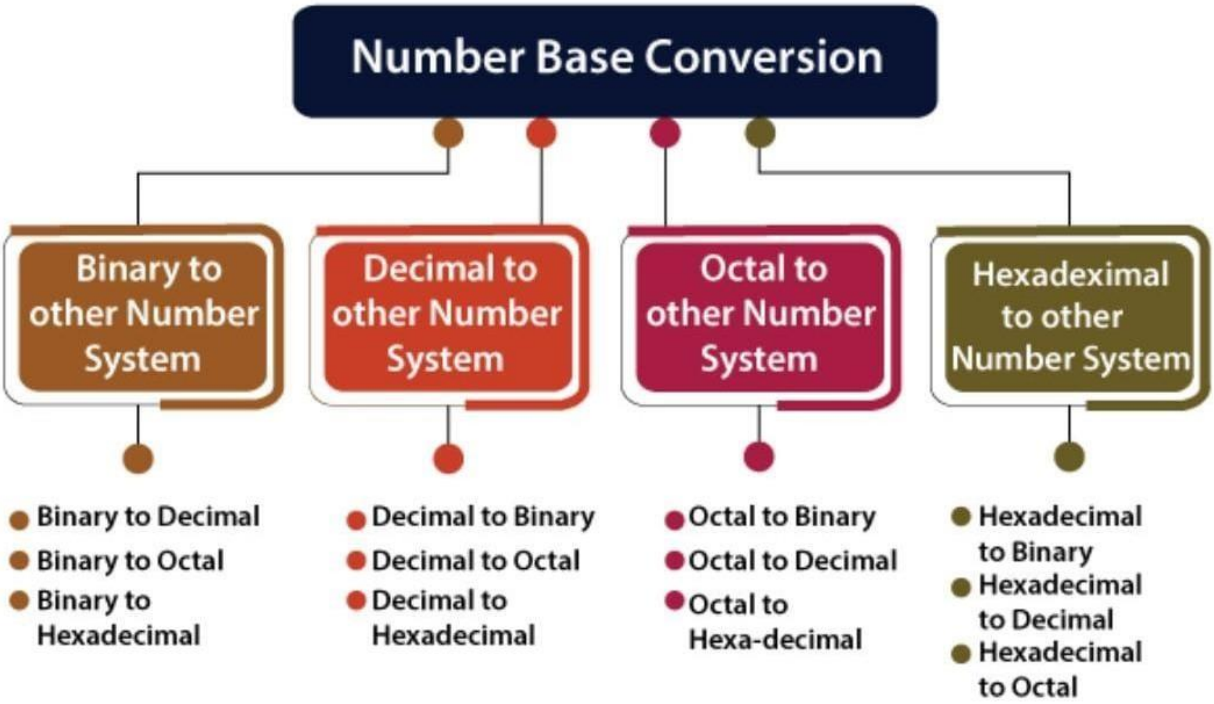
Binary Number	1	0	1	1	0	1	Decimal Number
Power of base	2^5	2^4	2^3	2^2	2^1	2^0	
Decimal equivalent	32	16	8	4	2	1	
Magnitude of each term	32	0	8	4	0	1	45

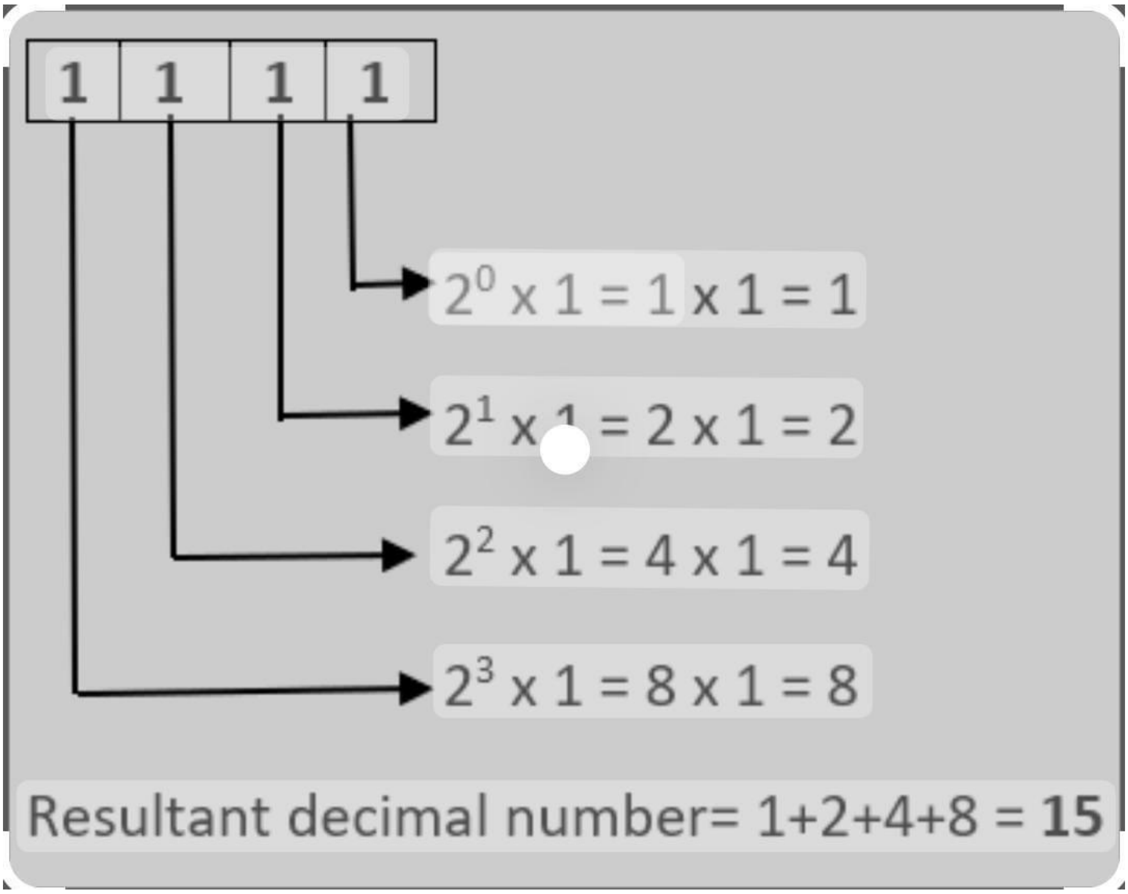
Octal Number System

- The base is 8.
- Symbols : 0, 1, 2, 3, 4, 5, 6, and 7.
- Positional weights :

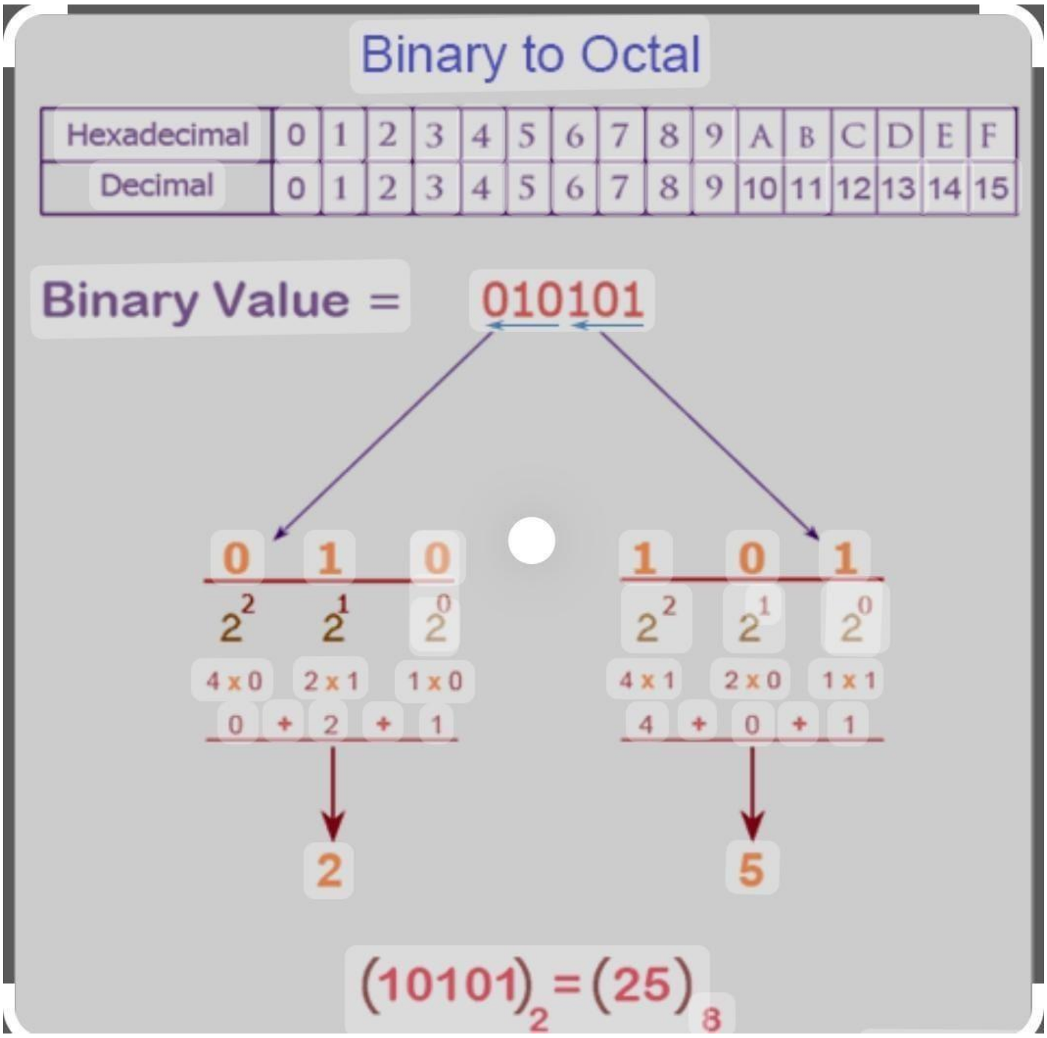
$8^0 = 1$	$8^{-1} = 1/8$
$8^1 = 8$	$8^{-2} = 1/64$
$8^2 = 64$	$8^{-3} = 1/256$
$8^3 = 256$	



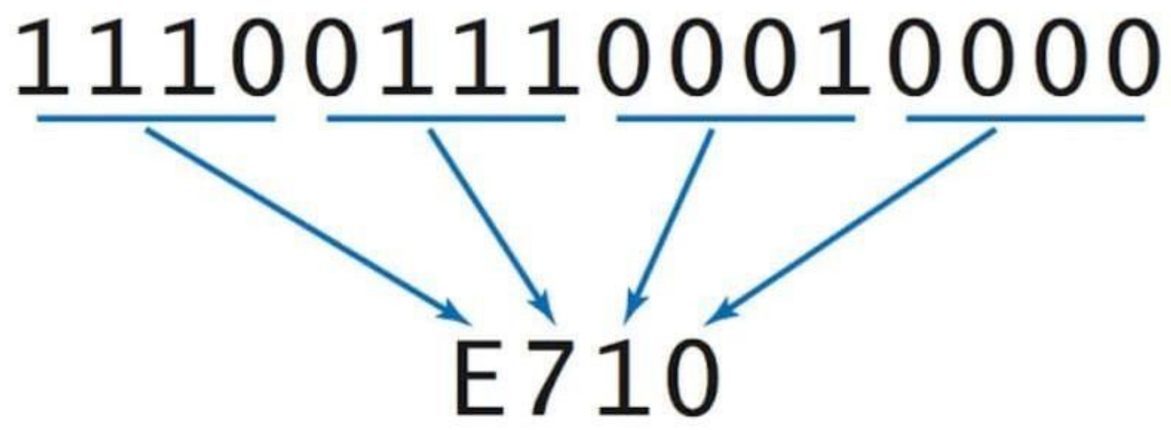

Number Base Conversion
Binary to other Number System
Decimal to other Number System
Octal to other Number System
Hexadeximal to other Number System
Binary to Decimal
Binary to Octal
Binary to Hexadecimal
Decimal to Binary
Decimal to Octal
Decimal to Hexadecimal
Octal to Binary
Octal to Decimal
Octal to Hexa-decimal
Hexadecimal to Binary
Hexadecimal to Decimal
Hexadecimal to Octal

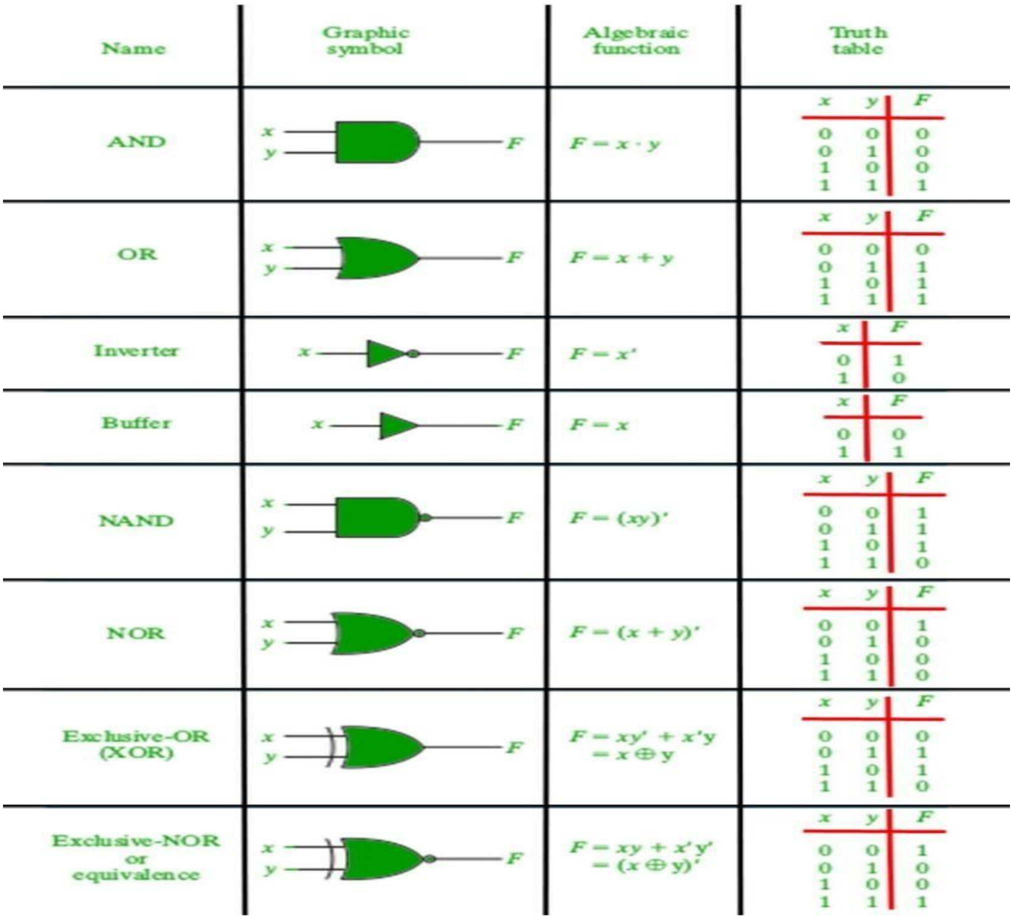

1 1 1 1
2^0 x 1 = 1 x 1 = 1
2^1 x 1 = 2 x 1 = 2
2^2 x 1 = 4 x 1 = 4
2^3 x 1 = 8 x 1 = 8
Resultant decimal number= 1+2+4+8 = 15

OCTAL	BINARY
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111



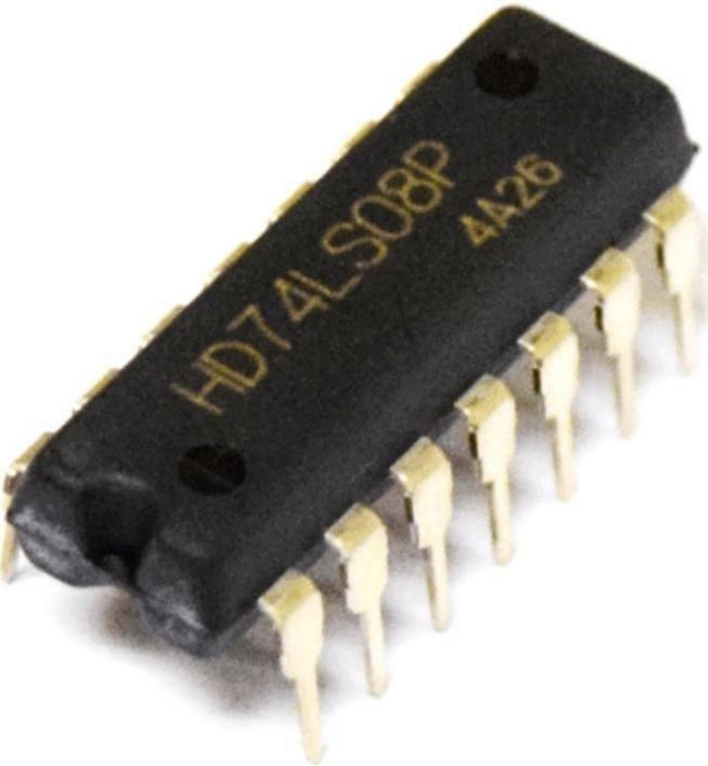
Decimal	Binary	Hexadecimal
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F

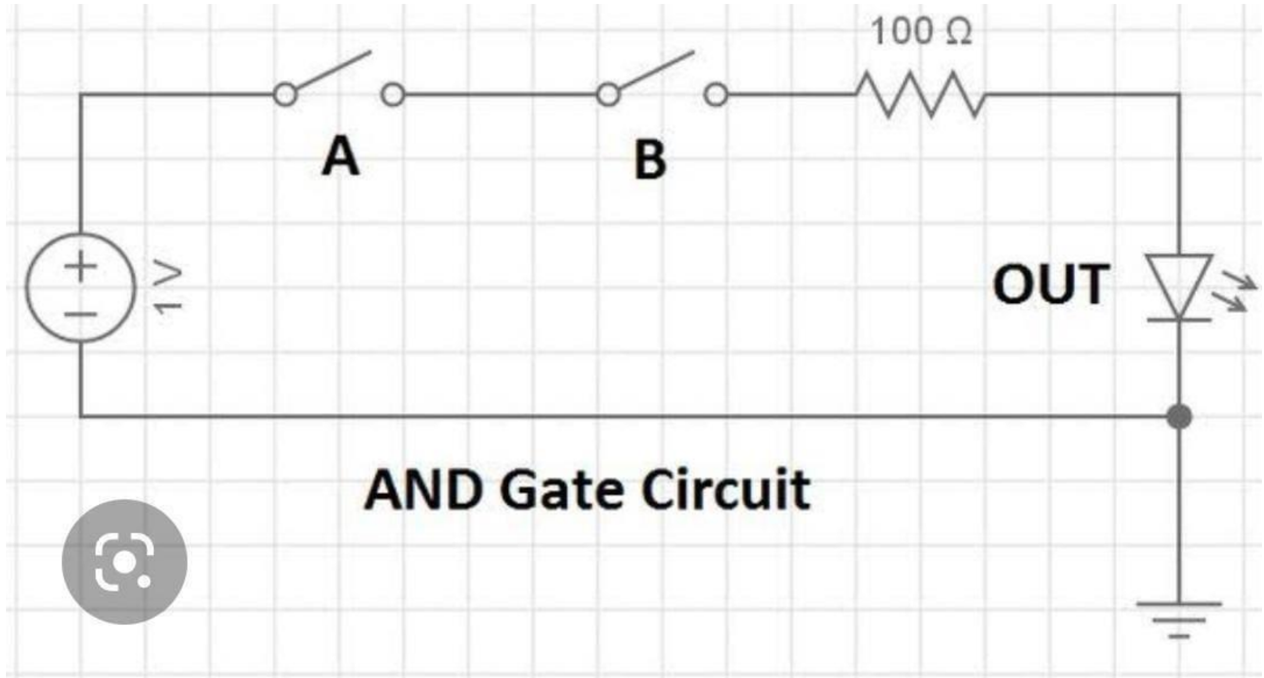




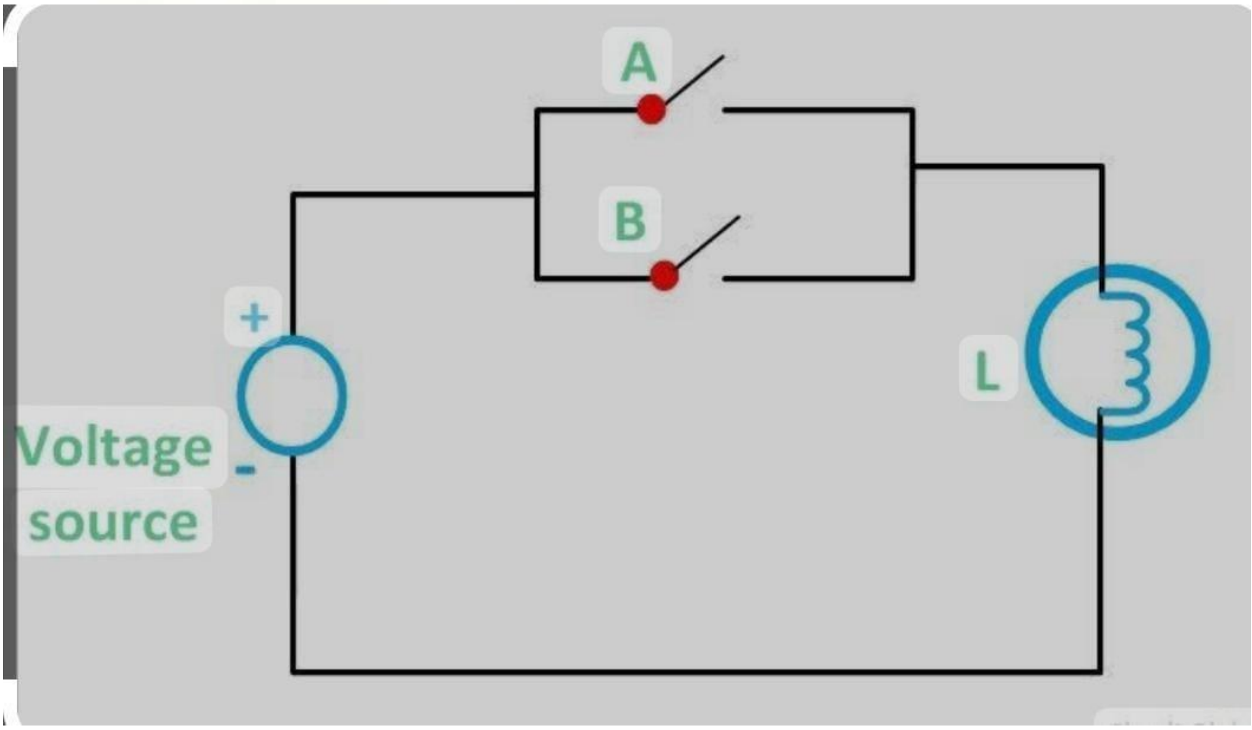
Name	Graphic symbol	Algebraic function	Truth table
AND	x, y → F	$F = x \cdot y$	x y | F 0 0 | 0 0 1 | 0 1 0 | 0 1 1 | 1
OR	x, y → F	$F = x + y$	x y | F 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 1
Inverter	x → F	$F = x'$	x | F 0 | 1 1 | 0
Buffer	x → F	$F = x$	x | F 0 | 0 1 | 1
NAND	x, y → F	$F = (xy)'$	x y | F 0 0 | 1 0 1 | 1 1 0 | 1 1 1 | 0
NOR	x, y → F	$F = (x + y)'$	x y | F 0 0 | 1 0 1 | 0 1 0 | 0 1 1 | 0
Exclusive-OR (XOR)	x, y → F	$F = xy' + x'y$ $= x \oplus y$	x y | F 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 0
Exclusive-NOR or equivalence	x, y → F	$F = xy + x'y'$ $= (x \oplus y)'$	x y | F 0 0 | 1 0 1 | 0 1 0 | 0 1 1 | 1

2-input AND gate

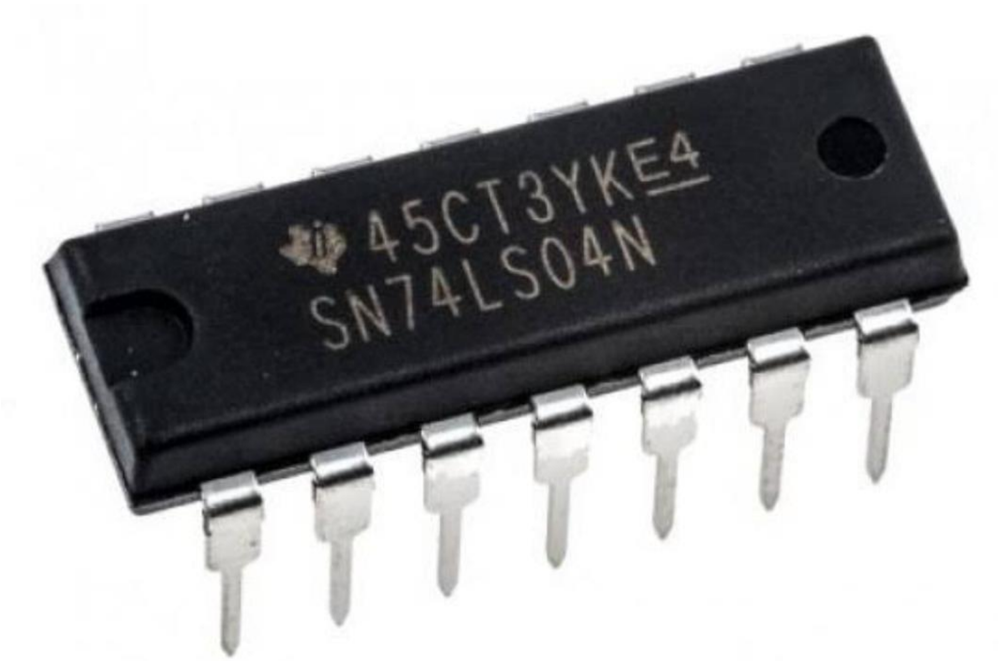




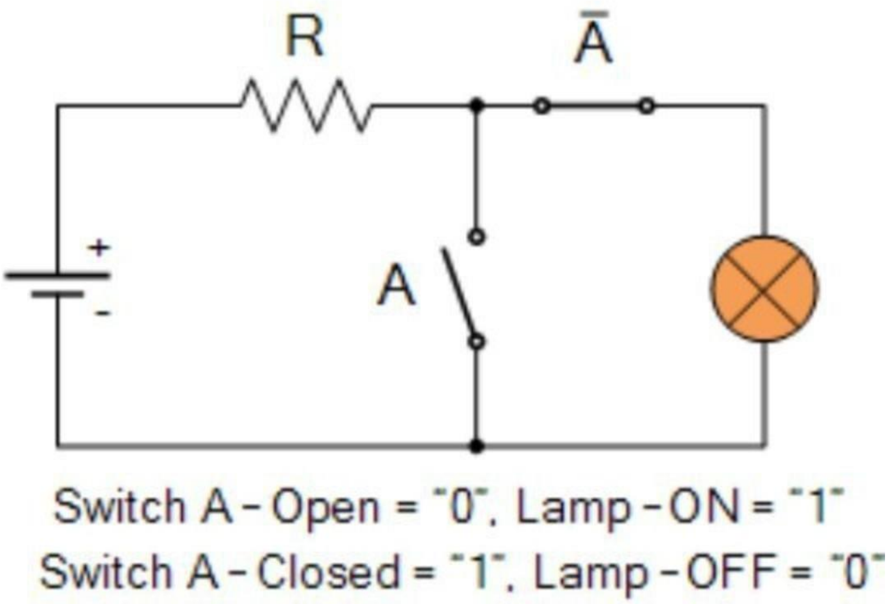
2-input OR gate



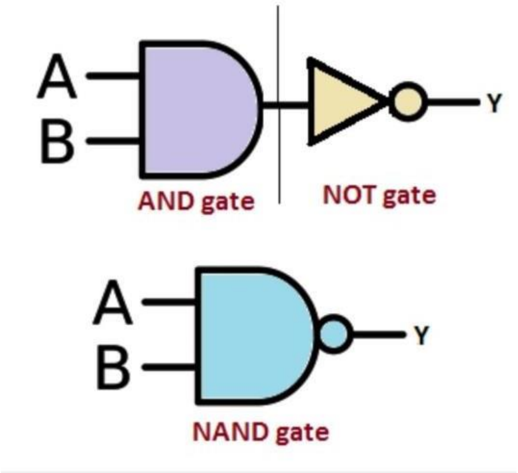
NOT gate

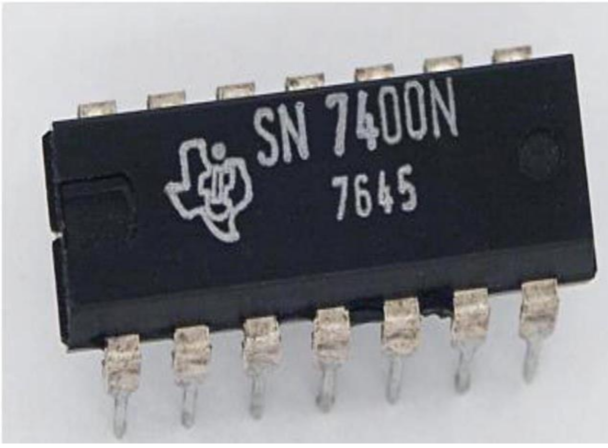


NOT Gate

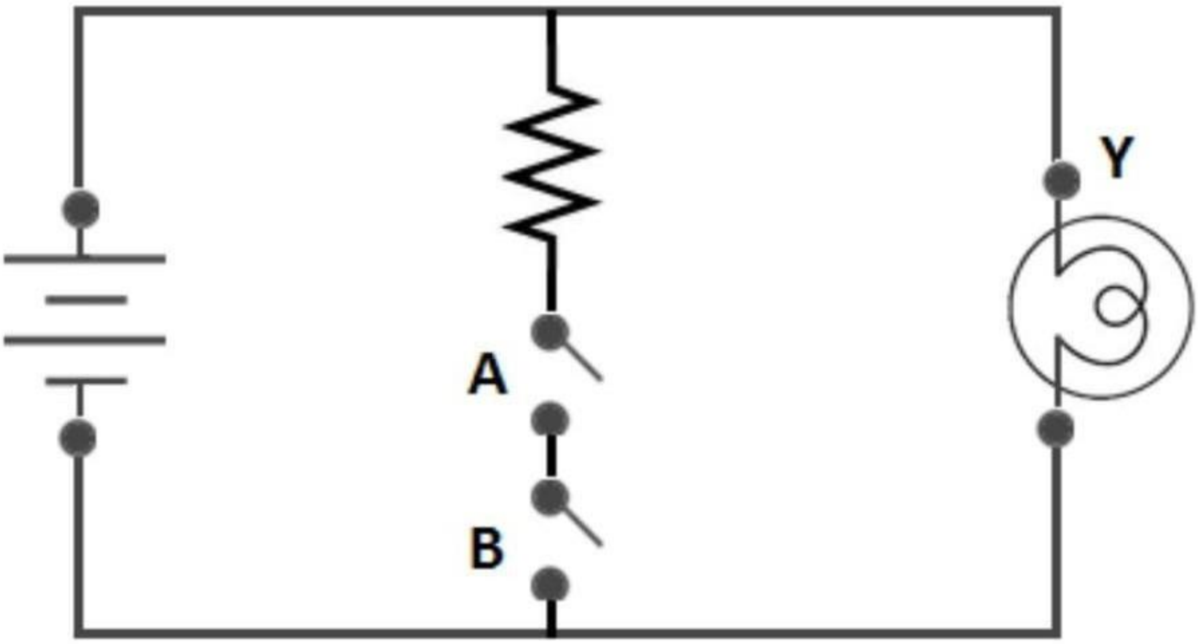


NAND GATE



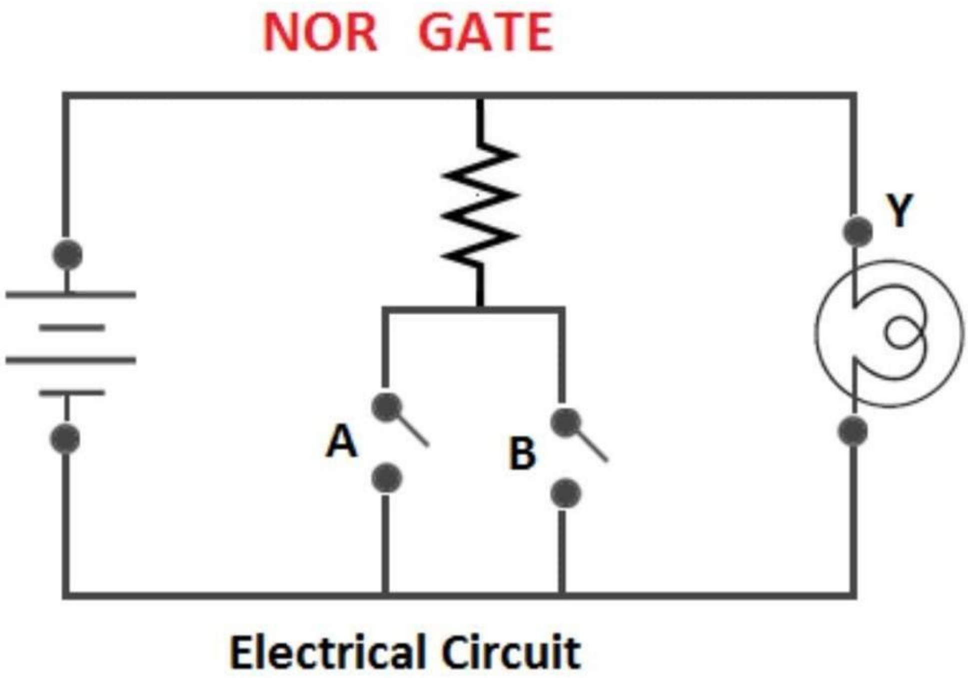


NAND GATE



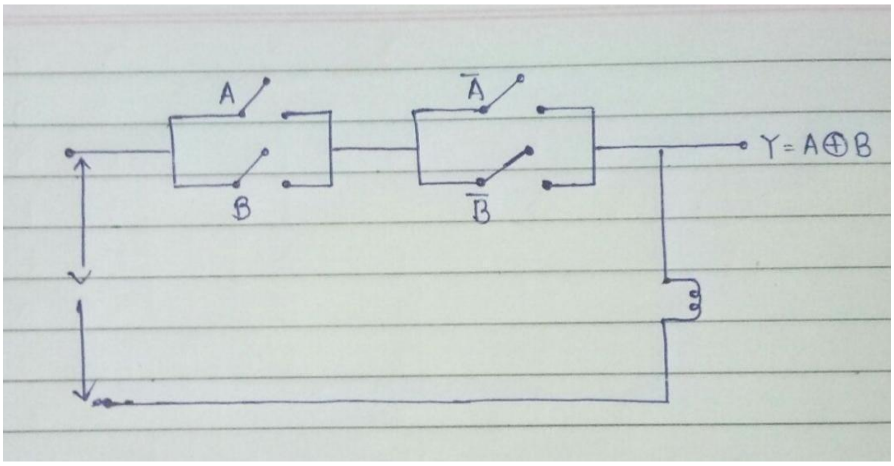
Electrical Circuit

NOR GATE

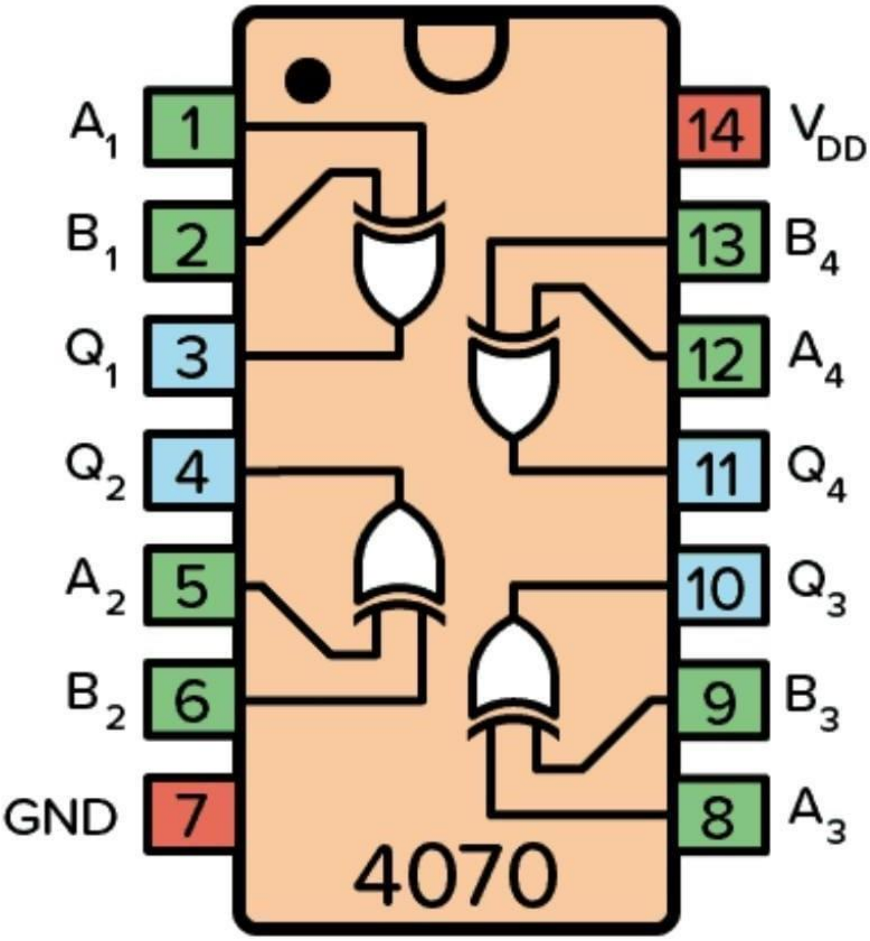


NOR Gate DIP14

EX-OR GATE

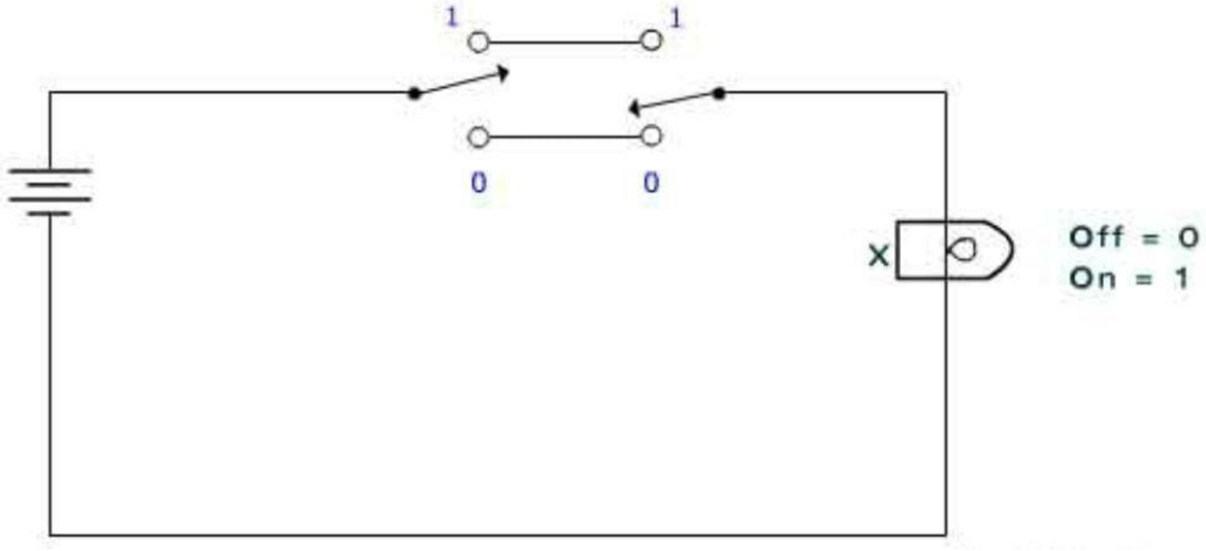


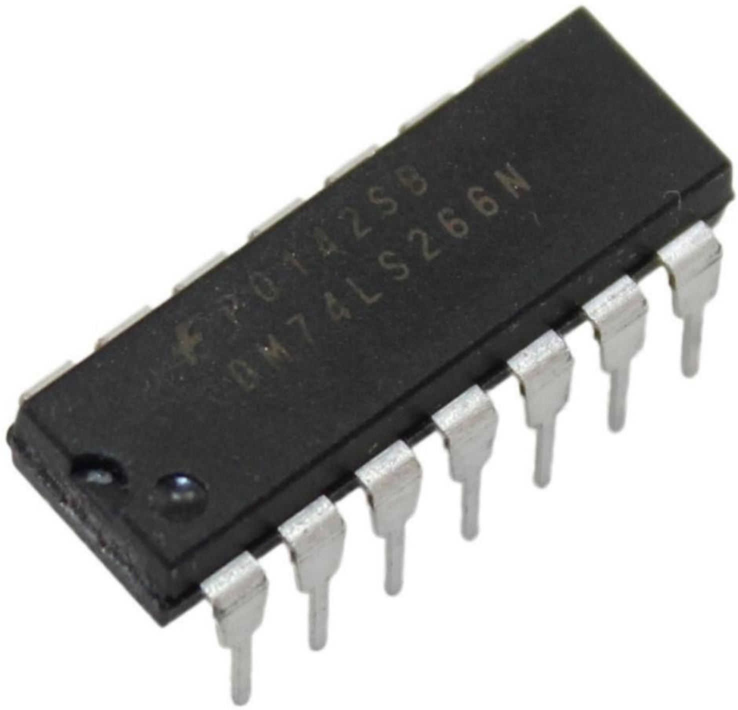
A
B
$\bar{A}$
$\bar{B}$
Y = A⊕B



A1
B1
Q1
Q2
A2
B2
GND
1
2
3
4
5
6
7
14
13
12
11
10
9
8
VDD
B4
A4
Q4
Q3
B3
A3
4070

EX-NOR GATE

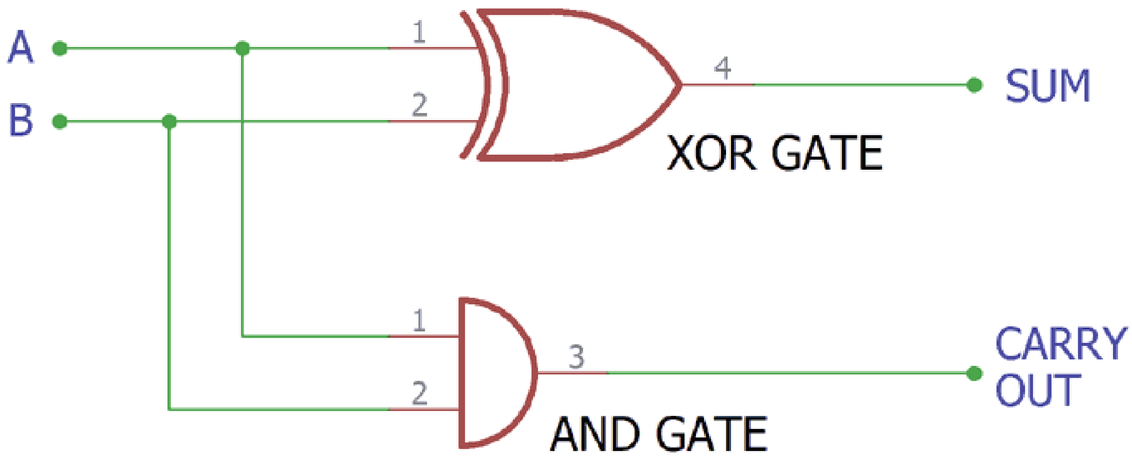

1
1
0
0
X
Off = 0
On = 1


DM74LS266N

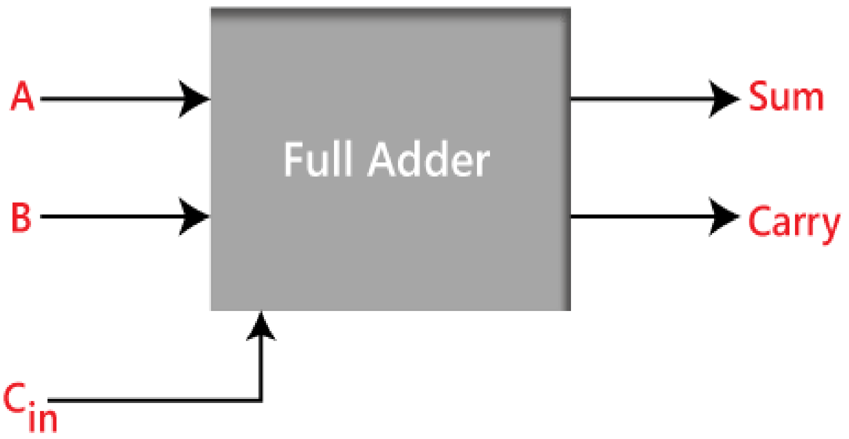
UNIT-2

COMBINATIONAL CIRCUITS

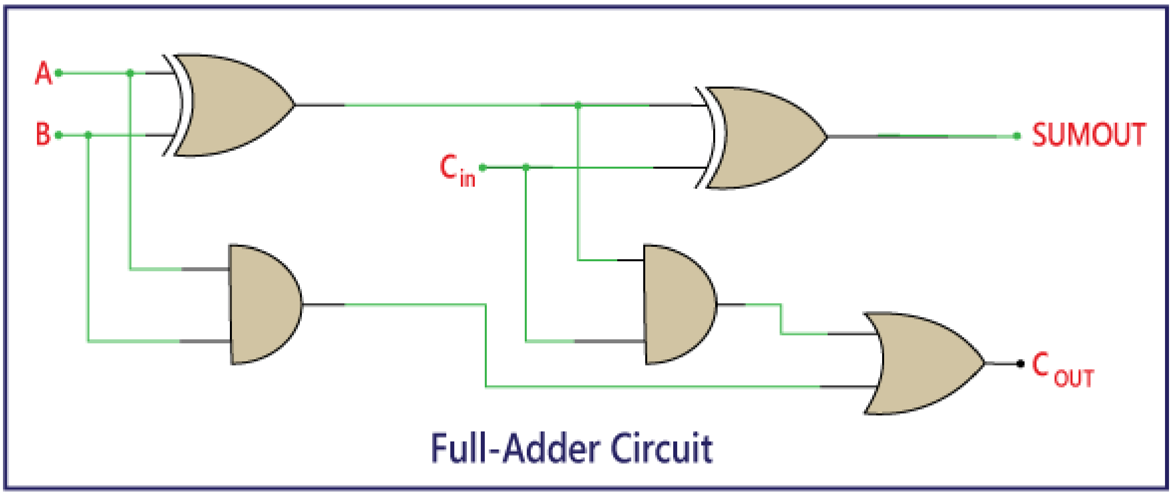
HALF ADDER

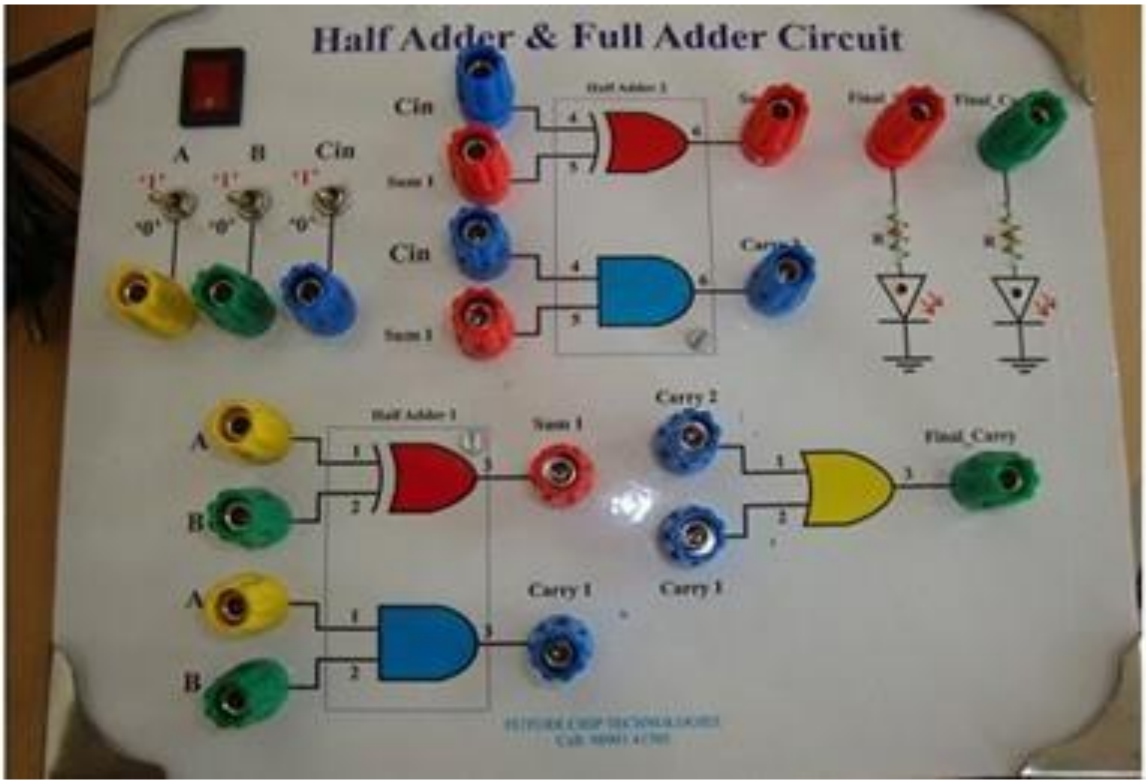


Truth Table			
Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

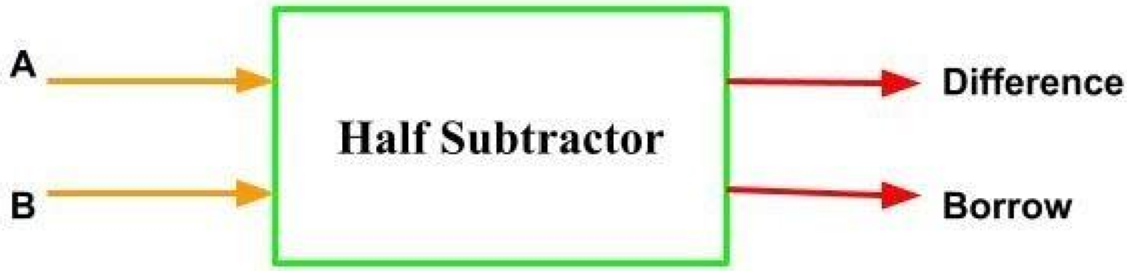


Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

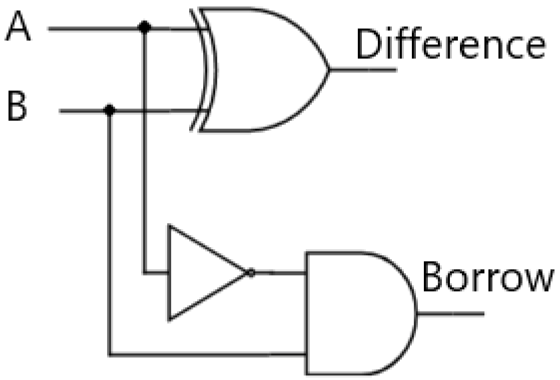




HALF SUBTRACTOR

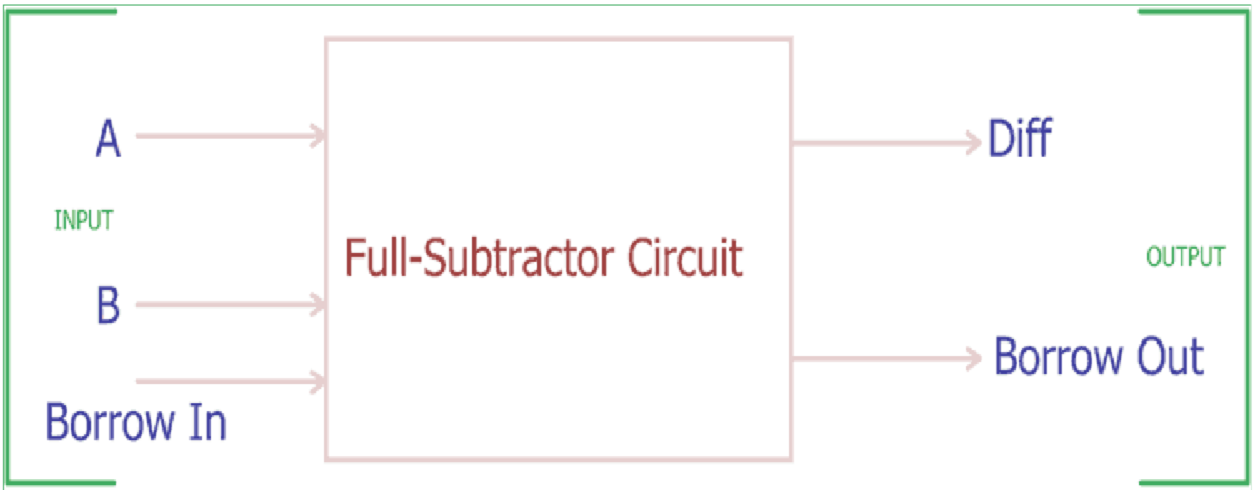


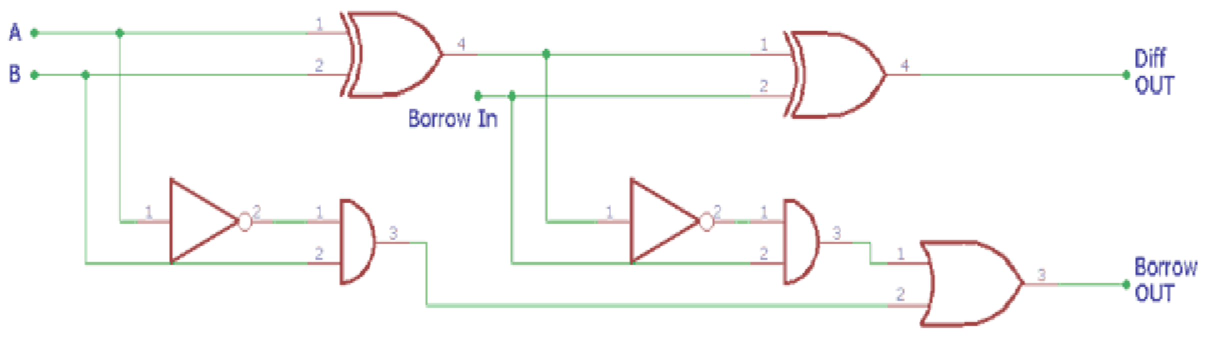
Inputs		Outputs	
A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0



FULL SUBTRACTOR

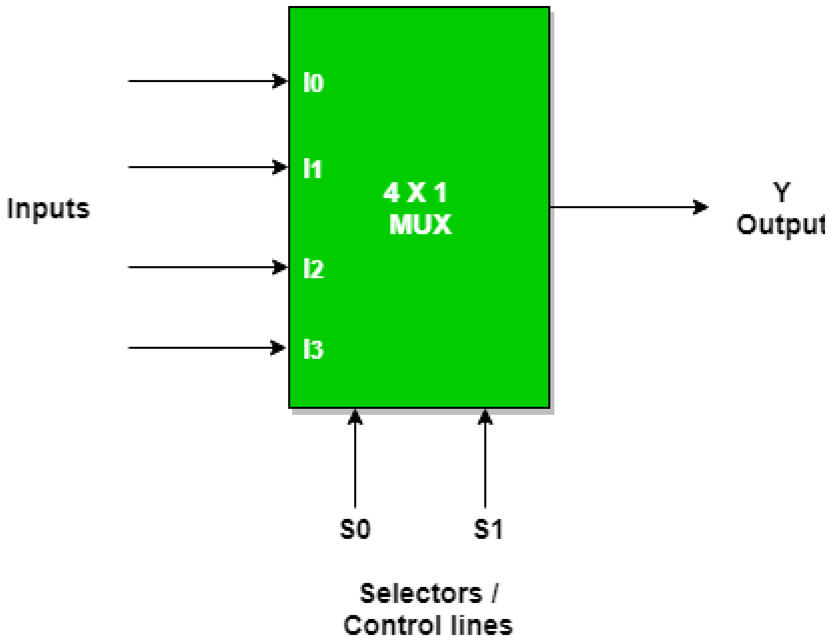
Full Subtractor-Truth Table				
Input			Output	
A	B	C	Difference	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1
www.flintgroups.com				





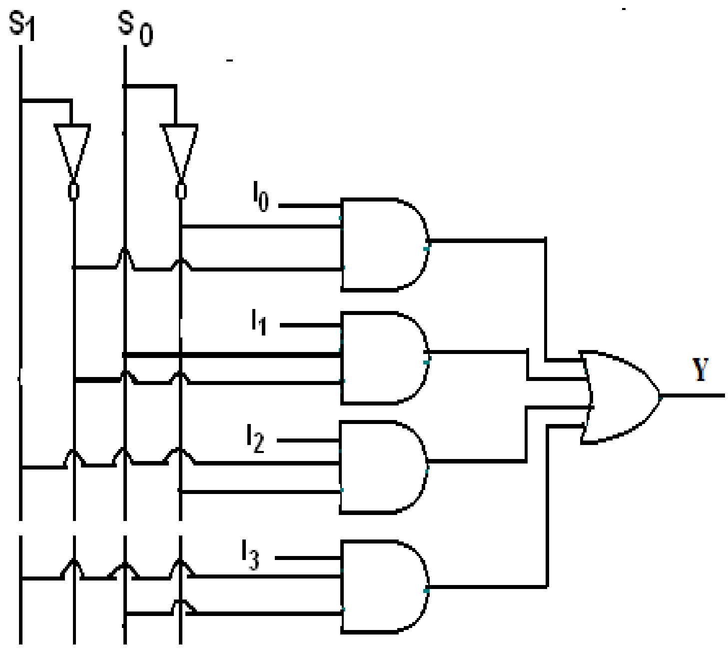
Full-Subtractor Circuit

4:1 MULTIPLEXER



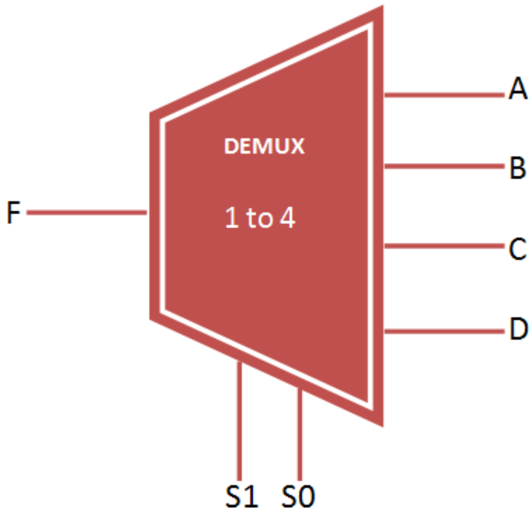
Input	S1	S0	Y
I_0	0	0	I_0
I_1	0	1	I_1
I_2	1	0	I_2
I_3	1	1	I_3

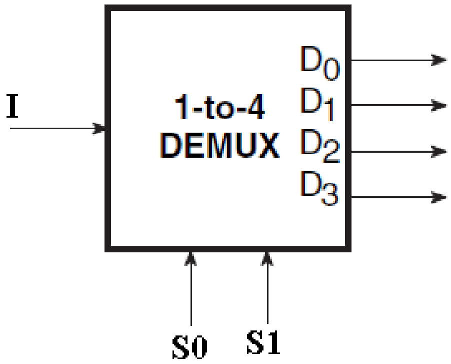
$$Y = S_1 S_0 I_3 + S_1 \overline{S_0} I_2 + \overline{S_1} S_0 I_1 + \overline{S_1}\,\overline{S_0} I_0$$



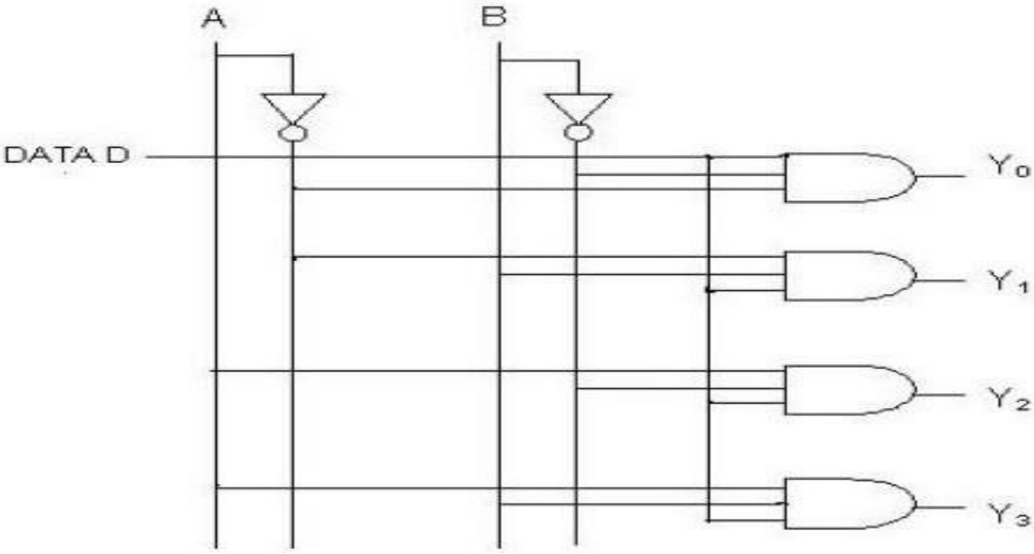
4 to 1 Multiplexer and its truth table

1:4 DEMULTIPLEXER

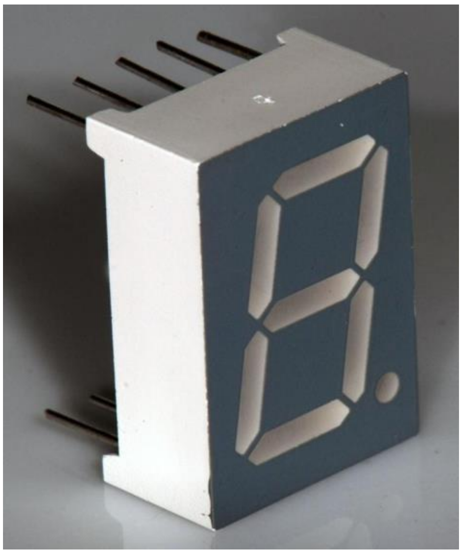


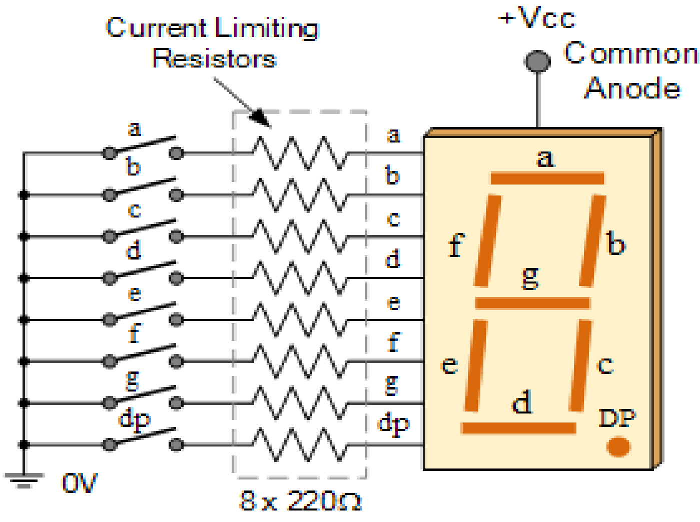


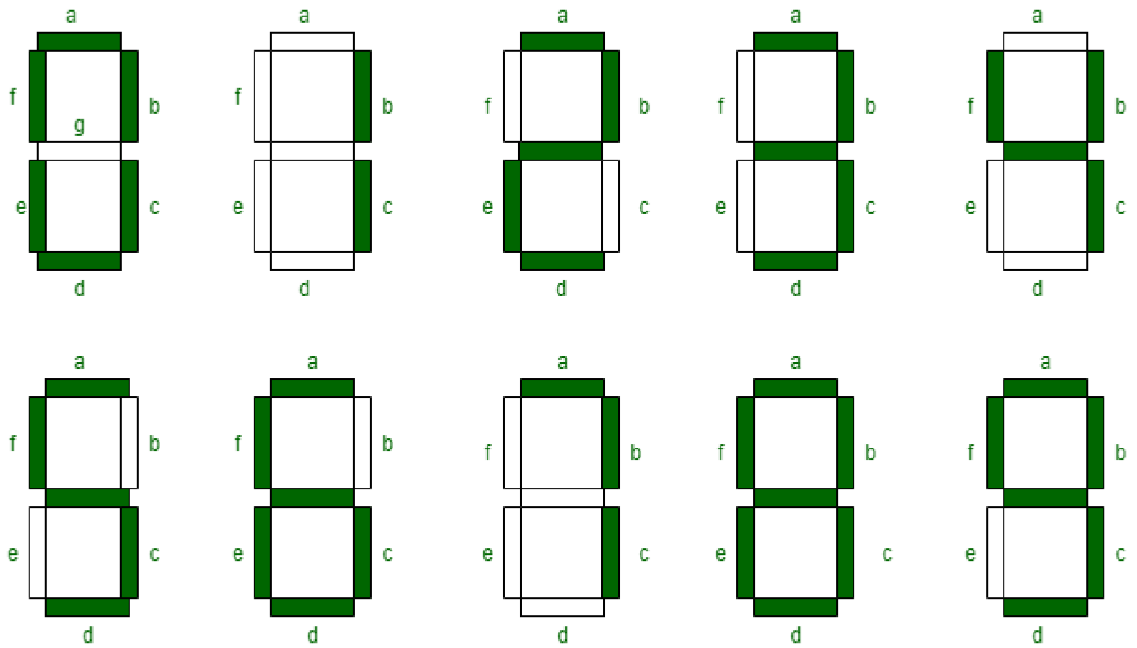
I	Select		O/P			
	S0	S1	D_0	D_1	D_2	D_3
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1



7 SEGMENT DISPLAY

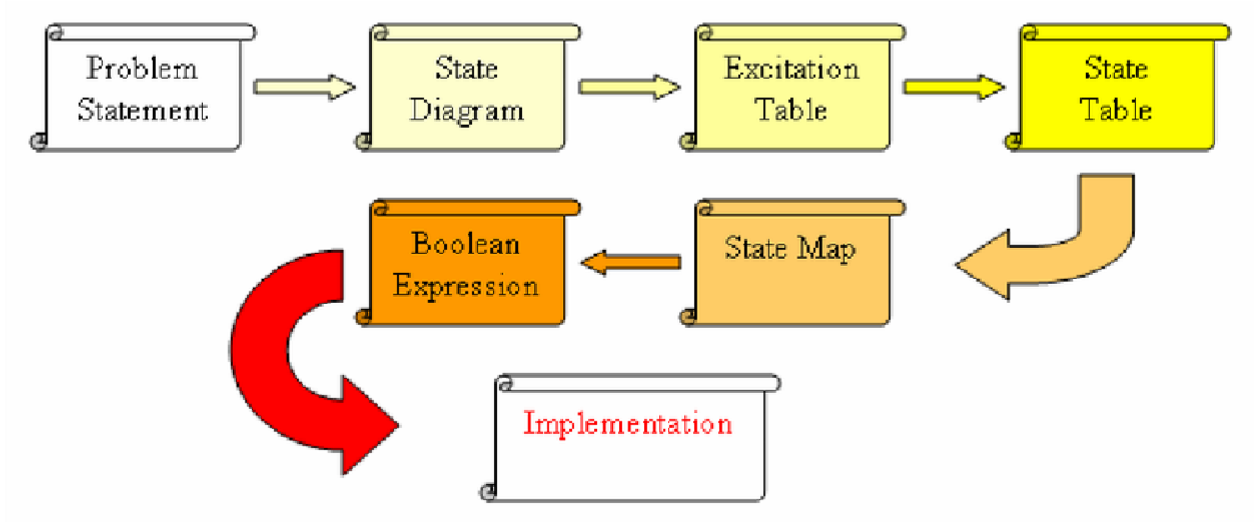


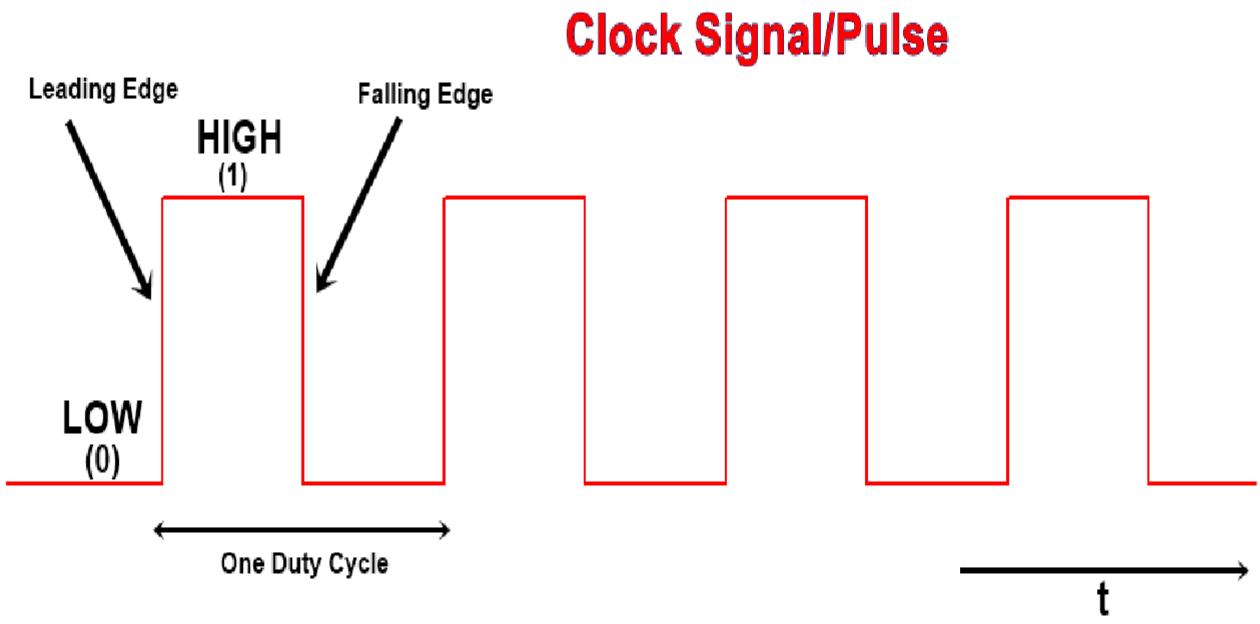


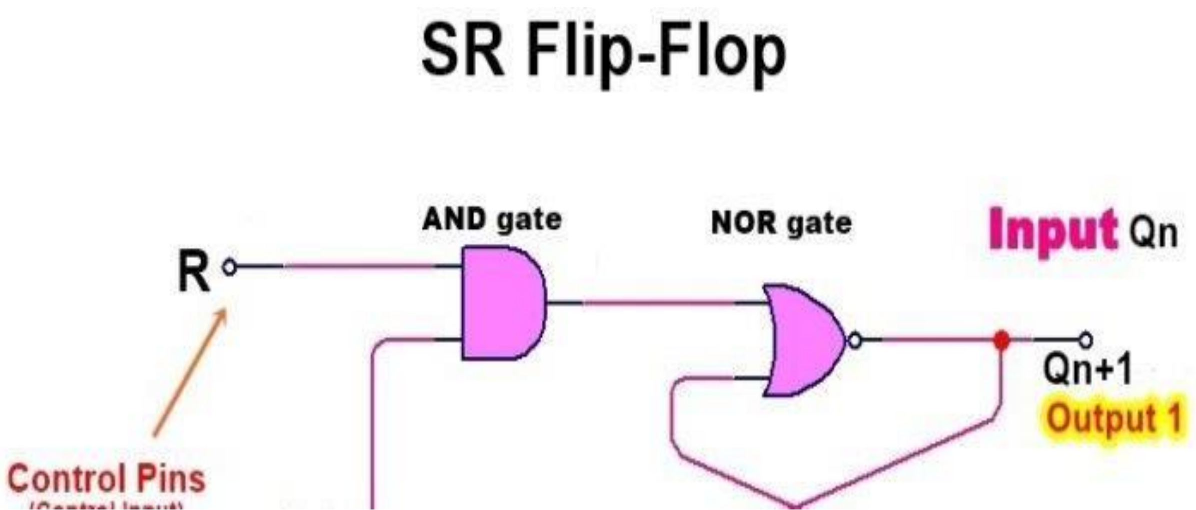


UNIT-3

SEQUENTIAL CIRCUIT

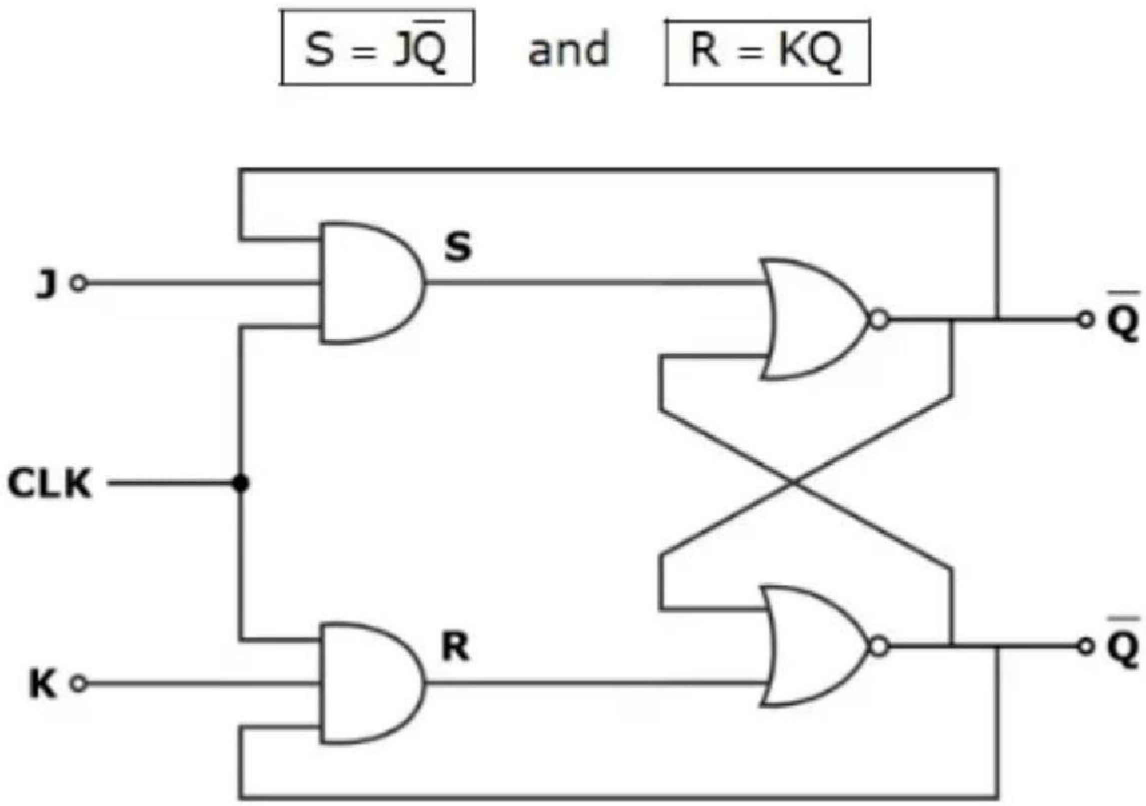




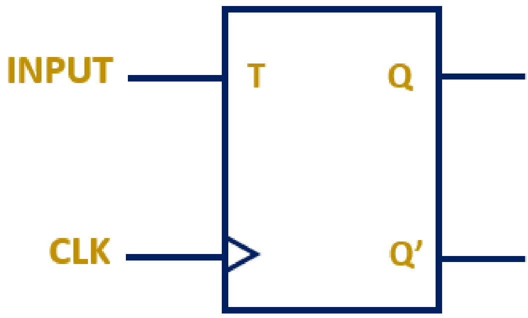


State	S	R	Q	Q'	Description
Set	1	0	0	1	Set Q'>>1
	1	1	0	1	No change
Reset	0	1	1	0	Reset Q'>>0
	1	1	1	0	No change
Invalid	0	0	1	1	Invalid Condition

JK Flip-Flop

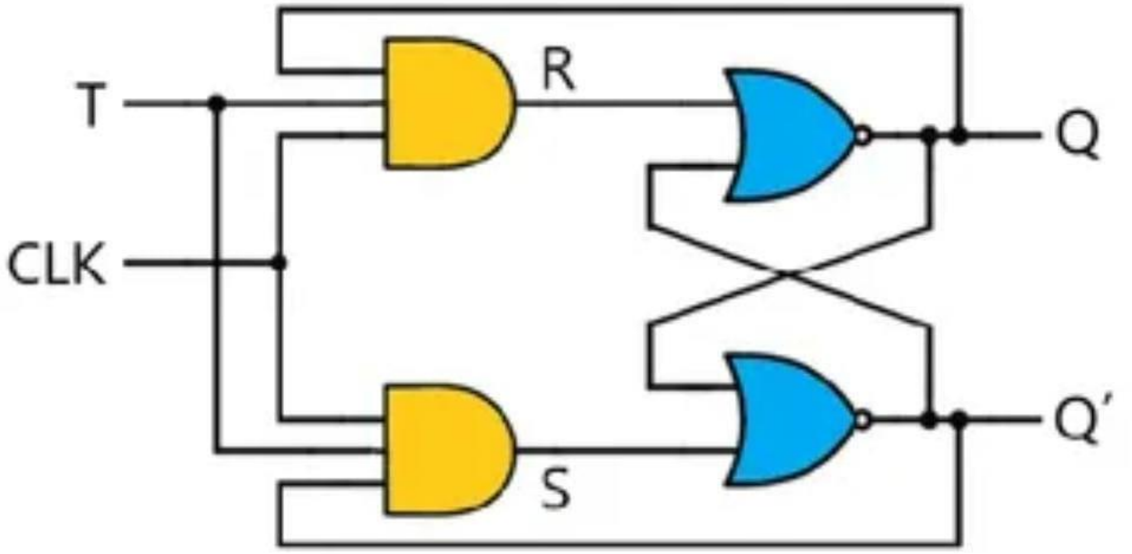


T Flip-Flop

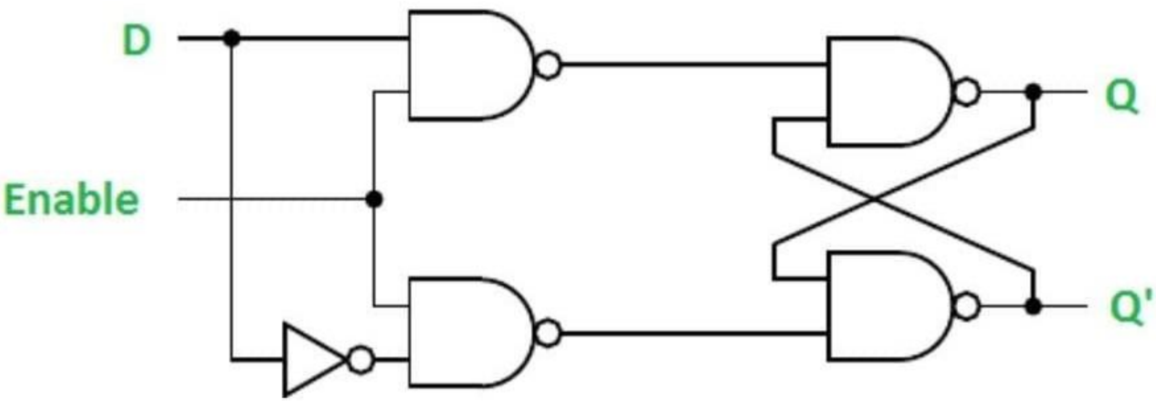


Clock	J	K	Q_{n+1}	State
0	x	x	Q_n	
1	0	0	Q_n	Hold
1	0	1	0	Reset
1	1	1	1	Set
1	1	1	$\overline{Q}_n$	Toggle

T FLIP-FLOP



D FLIP-FLOP



Truth Table for the D-type Flip Flop

Clock	D	Q	Q'	Description
↓ » 0	X	Q	Q'	Memory no change
↑ » 1	0	0	1	Reset Q » 0
↑ » 1	1	1	0	Set Q » 1

Symbols ↓ and ↑ indicates the direction of the clock pulse. D-type flip flop assumed these symbols as edge-triggers.