GANDHI SCHOOL OF ENGINEERING
BHABANDHA, BERHAMPUR
SESSION PLAN
3RD SEMESTER, BRANCH-INFORMATION TECHNOLOGY

DIGITAL ELECTRONICS (TH-3)

Name of the Faculty –ER. SURABHI TRIPATHY

Topics to be taken				TOPIC NO.	Actually Taken		
SL NO & CHAPTER	No. of Periods assigned by SCTE & VT	Details of the topics	PLANNING DATE		Details of the topics	ACTUAL DATE	Remarks
1 Basics of Digital Electronics	12	**Basics of Digital Electronics** 1.1 Number System-Binary, Octal, Decimal, Hexadecimal - Conversion from one system to another number system. 1.2 Arithmetic Operation-Addition, Subtraction, Multiplication, Division, 1"s & 2"s complement of Binary numbers& Subtraction using complements method 1.3 Digital Code & its application & distinguish between weighted & non-weight Code, Binary codes, excess-3 and Gray codes. 1.4 Logic gates: AND, OR, NOT, NAND, NOR, Exclusive-OR, Exclusive-NOR--Symbol, Function, expression, truth table & timing diagram 1.5 Universal Gates& its Realisation 1.6 Boolean algebra, Boolean expressions, Demorgan"s Theorems. 1.7 Represent Logic Expression: SOP & POS forms 1.8 Karnaugh map (3 & 4 Variables)&Minimization of logical expressions ,don't care conditions	03-07-2024 TO 31-07-2024	1 1.1 1.2 1.3 1.4 1.5 1.6 1.7 1.8	**Basics of Digital Electronics** INTRODUCTION 1.1 Number System-Binary, Octal, Decimal, Hexadecimal - Conversion from one system to another number system. 1.2 Arithmetic Operation-Addition, Subtraction, Multiplication, Division, 1"s & 2"s complement of Binary numbers & Subtraction using complements method 1.3 Digital Code & its application & distinguish between weighted & non-weight Code, Binary codes, excess-3 and Gray codes. 1.4 Logic gates: AND, OR, NOT, NAND, NOR, Exclusive-OR, Exclusive-NOR--Symbol, Function, expression, truth table & timing diagram 1.5 Universal Gates& its Realisation 1.6 Boolean algebra, Boolean expressions, Demorgan"s Theorems. 1.7 Represent Logic Expression: SOP & POS forms 1.8 Karnaugh map (3 & 4 Variables)& Minimization of logical expressions ,don't care conditions	07-03-2024 07-04-2024 07-06-2024 07-10-2024 13-07-2024 18-07-2024 20-07-2024 22-07-2024 25-07-2024 27-07-2024 29-07-2024 31-07-2024	

2 Combinational Logic Circuits	12	**Combinational Logic Circuits** 2.1 Half adder, Full adder, Half Subtractor, Full Subtractor, Serial and Parallel Binary 4 bit adder. 2.2 Multiplexer (4:1), De- multiplexer (1:4), Decoder, Encoder, Digital comparator (3 Bit) 2.3 Seven segment Decoder (Definition, relevance, gate level of circuit Logic circuit, truth table, Applications of above)	01-08-2024 TO 31-08-2024	2 2.1 2.2 2.3	**Combinational Logic Circuits INTRODUCTION** 2.1 Half adder, Full adder, . Half Subtractor, Full Subtractor , Serial and Parallel Binary 4 bit adder 2.2 Multiplexer (4:1), , De- multiplexer (1:4) Decoder, Encoder ,Digital comparator (3 Bit) 2.3 Seven segment Decoder-Definition Seven segment Decoder relevance , gate level of circuit Logic circuit , truth table, Applications of above	01-08-2024 03-08-2024 05-08-2024 07-08-2024 10-08-2024 12-08-2024 14-08-2024 17-08-2024 22-08-2024 24-08-2024 29-08-2024 31-08-2024	
3 Sequential Logic Circuits	12	**Sequential Logic Circuits** 3.1 Principle of flip-flops operation, its Types, 3.2 SR Flip Flop using NAND, NOR Latch (un clocked). 3.3 Clocked SR,D,JK,T,JK Master Slave flip-flops-Symbol, logic Circuit, truth table and applications 3.4 Concept of Racing and how it can be avoided	04-09-2024 TO 21-10-2024	3 3.1 3.2 3.3 3.4	**Sequential Logic Circuits- INTRODUCTION** Sequential Logic Circuits- INTRODUCTION 3.1 Principle of flip-flops operation,its Types, flip-flops operationS, its Types, 3.2 SR Flip Flop using NAND, SR Flip Flop using NAND NOR Latch (un clocked). 3.3 Clocked SR,D,JK,T,JK flip-flops-Symbol Master Slave flip-flops-Symbol, logic Circuit, truth table and applications 3.4 Concept of Racing and how it can be avoided Concept of Racing and how it can be avoided	04-09-2024 09-09-2024 11-09-2024 14-09-2024 18-09-2024 21-09-2024 25-09-2024 26-09-2024 03-10-2024 05-10-2024 07-10-2024 21-10-2024	
4 Registers, Memories & PLD	8	**Registers, Memories & PLD** 4.1 Shift Registers-Serial in Serial -out, Serial- in Parallel-out, Parallel in serial out and Parallel in parallel out 4.2 Universal shift registers-Applications 4.3 Types of Counter & applications 4.4 Binary counter, Asynchronous ripple counter (UP & DOWN), Decade counter. Synchronous counter, Ring Counter. 4.5 Concept of memories-RAM, ROM, static RAM, dynamic RAM,PS RAM 4.6 Basic concept of PLD & applications	26-10-2024 TO 16-11-2024	4 4.1 4.2 4.3 4.4 4.5 4.6	**Registers,Memories & PLD INTRODUCTION** 4.1 Shift Registers-Serial in Serial -out, Serial-in Parallel-out, Parallel in serial out and Parallel in parallel out 4.2 Universal shift registers-Applications 4.3 Types of Counter & applications 4.4 Binary counter, Asynchronous ripple counter (UP & DOWN), Decade counter. Synchronous counter, Ring Counter. 4.5 Concept of memories-RAM, ROM, static RAM, dynamic RAM,PS RAM 4.6 Basic concept of PLD & applications	26-10-2024 30-10-2024 02-11-2024 06-11-2024 07-11-2024 09-11-2024 11-11-2024 16-11-2024	

5 A/D and D/A Converters	7	**A/D and D/A Converters** 5.1 Necessity of A/D and D/A converters. 5.2 D/A conversion using weighted resistors methods. 5.3 D/A conversion using R-2R ladder (Weighted resistors) network. 5.4 A/D conversion using counter method. 5.5 A/D conversion using Successive approximate method	18-11-2024 TO 30-11-2024	5 5.1 5.2 5.3 5.4 5.5	**A/D and D/A Converters-INTRODUCTION** 5.1 Necessity of A/D and D/A converters. Necessity of A/D and D/A converters. 5.2 D/A conversion using weighted resistors methods. 5.3 D/A conversion using R-2R ladder (Weighted resistors) network. 5.4 A/D conversion using counter method. 5.5 A/D conversion using Successive approximate method	18-11-2024 20-11-2024 21-11-2024 25-11-2024 27-11-2024 28-11-2024 30-11-2024	
6 LOGIC FAMILIES	9	**LOGIC FAMILIES** 6.1 Various logic families &categories according to the IC fabrication process 6.2 Characteristics of Digital ICs-Propagation Delay, fan-out, fan-in, Power Dissipation ,Noise Margin ,Power Supply requirement &Speed with Reference to logic families. 6.3 Features, circuit operation &various applications of TTL(NAND), CMOS (NAND & NOR)	02-12-2024 TO 16-12-2024	6 6.1 6.2 6.3	**LOGIC FAMILIES-INTRODUCTION** 6.1 Various logic families & categories according to the IC fabrication process 6.2 Characteristics of Digital ICs-Propagation Delay, fan-out, fan-in, Power Dissipation ,Noise Margin ,Power Supply requirement &Speed with Reference to logic families. 6.3 Features, circuit operation & various applications of TTL(NAND), CMOS (NAND & NOR)	02-12-2024 04-12-2024 05-12-2024 07-12-2024 09-12-2024 11-12-2024 12-12-2024 14-12-2024 16-12-2024	

CLASS COVERED BY

HOD, INFORMATION TECHNOLOGY