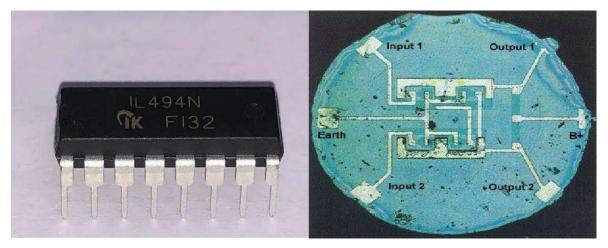
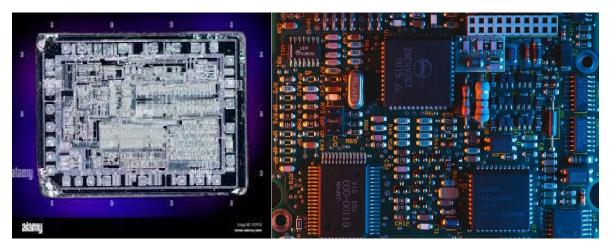
# TEACHING LEARNING MATERIAL OF VLSI & EMBEDDED SYSTEM

PREPARED BY:ER.PRETESSHA MAHAPATRO & ER. S.K BISOYEE



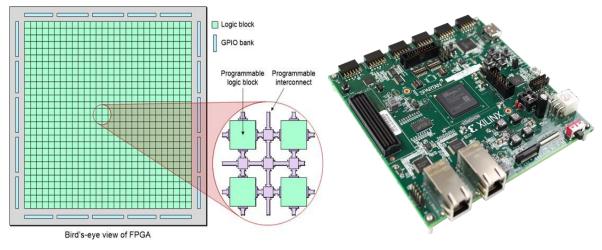
SINGLE MONOLITHIC CHIP (IC)

FIRST MONOLITHIC CHIP



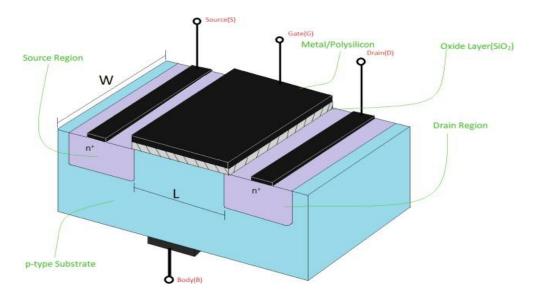
IC

PHYSICAL DESIGN OF VLSI

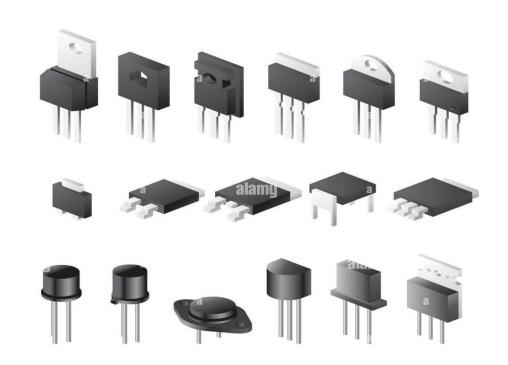


CONFIGURABLE LOGIC BLOCKS OF FPGA SPARTAN-7

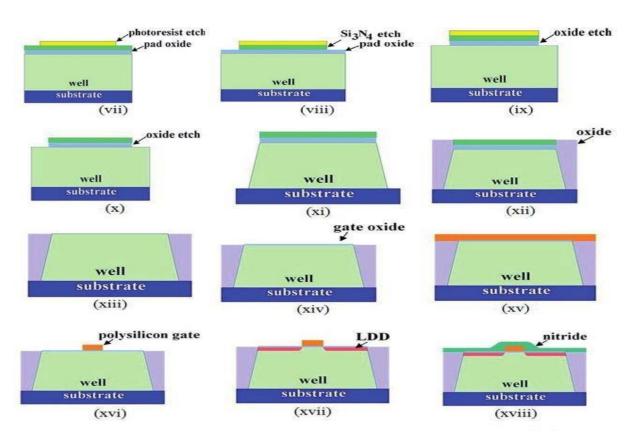
**FPGA** 



MOS TRANSISTOR STRUCTURE



DIFFERENT TYPES OF MOSFET



**FABRICATION PROCESS** 

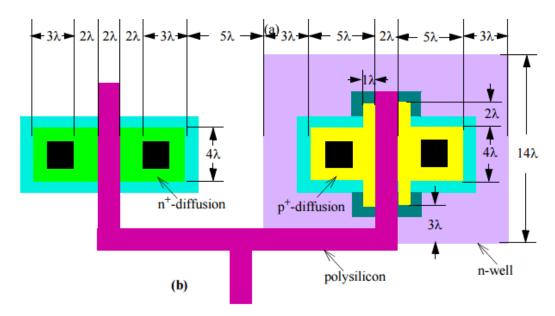
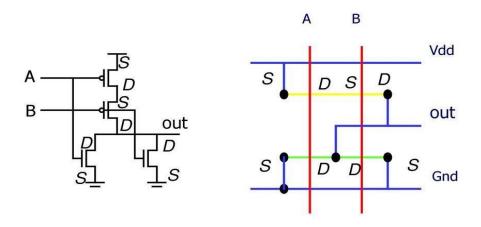


Figure 1 (a)Electrical model of a cascade connection of twoCMOS inverters. (b)A partial sketch of a CMOS inverter layout (metal layer not shown).

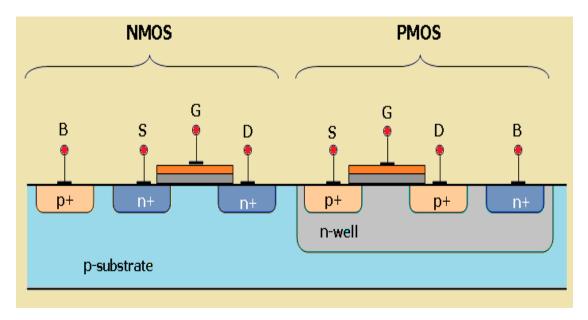
#### LAYOUT DESIGN

# Stick Diagram for CMOS NOR

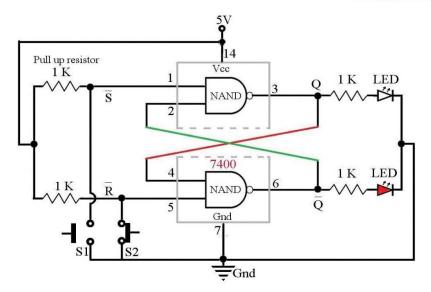


20 Combinational Circuits

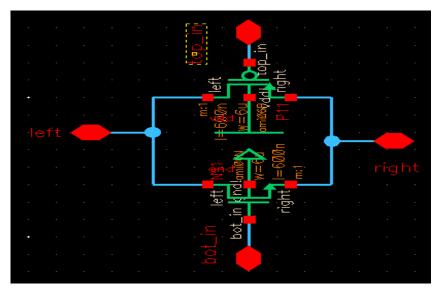
STICK DIAGRAM



CMOS



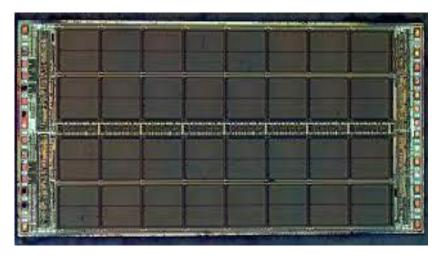
SR LATCH USING NAND GATE



TRANSMISSION GATE



**DRAM** 



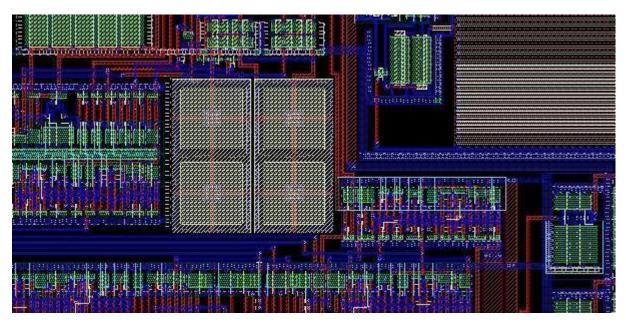
TYPICAL COFIGURATION OF DRAM CHIP



SRAM



FLASH MEMORY



#### **EDA TOOL SIMULATION**

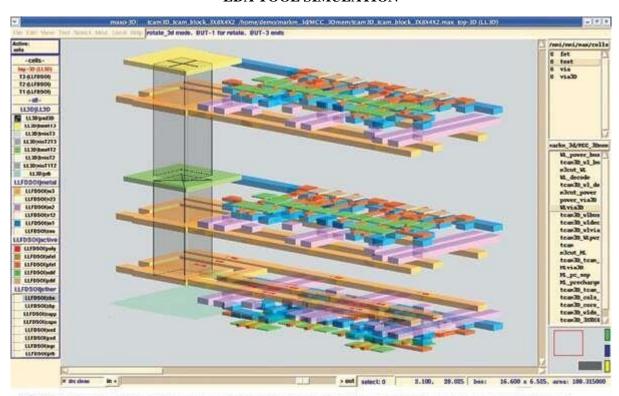


Figure 5 The Max-3D tool incorporates features for 3-D-design methods, so you can organize and manage design data for every wafer level in a stacked design.

#### **3-D STRUCTURE IC DESIGN**



## RASBERRY PI





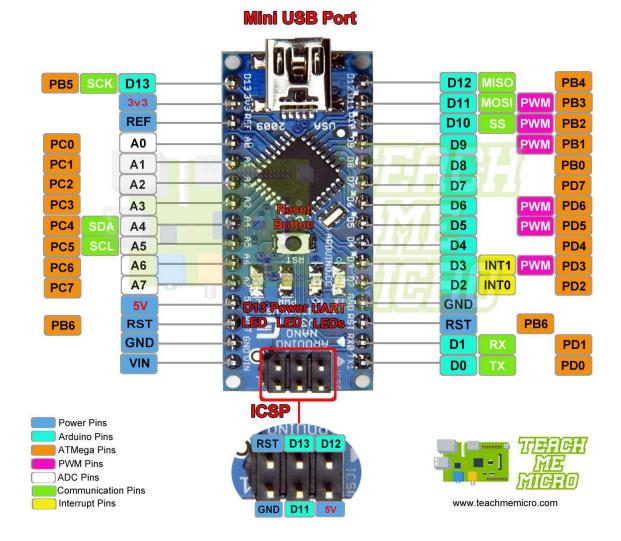
ARDUINO UNO

ARDUINO ROBOT

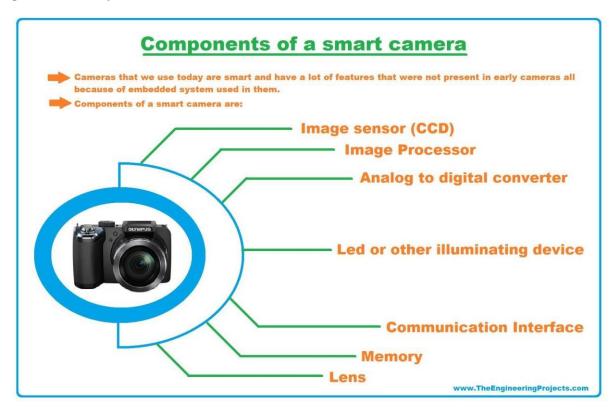


ARDUINO MICRO

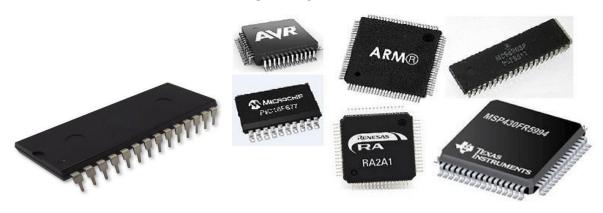
# **ARDUINO NANO PINOUT**



**ARDUINO NANO** 



#### **DIGITAL CAMERA**



8-BIT MICROCONTROLLER

DIFFERENT TYPE OF MICROCONTROLLERS