GANDHI SCHOOL OF ENGINEERING

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DEMP LAB MANUAL (5TH SEM, ELECTRICAL)

EXPERIMENT NO. 01

Aim of the Experiment

To study digital ICs 7400, 7402, 7404, 7408, 7432 and 7486 using a digital trainer kit.

Apparatus Required

- Digital trainer kit
- Patch cords or wires
- ICs (7400, 7402, 7404, 7408, 7432, 7486)

Theory

IC 7400

This is a NAND gate IC having fourteen pins. Power supply is given to pin no. 14 and pin no. 7 is grounded; the other pins represent inputs and outputs.

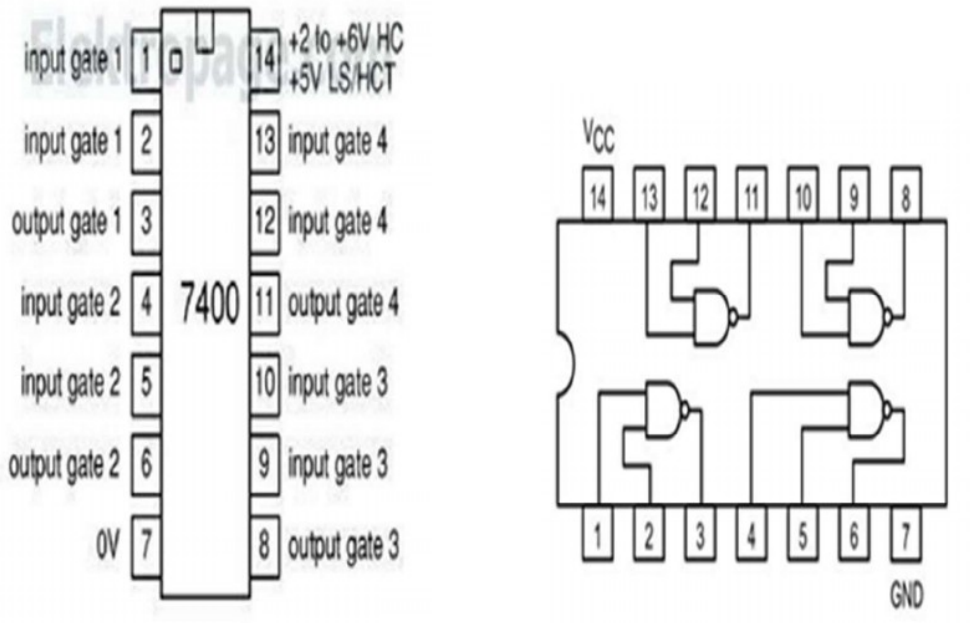


Fig.: Pin diagram of IC 7400 (Quad 2-input NAND gate)

IC 7402

This is a NOR gate IC having fourteen pins. Power supply is given to pin no. 14 and pin no. 7 is grounded; the other pins represent inputs and outputs.

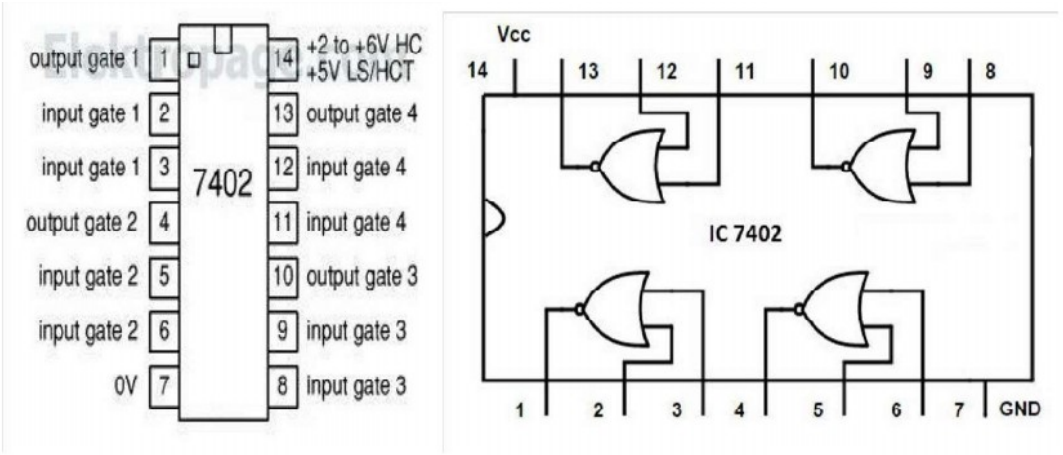


Fig.: Pin diagram of IC 7402 (Quad 2-input NOR gate)

IC 7404

This is a NOT gate IC having fourteen pins. Power supply is given to pin no. 14 and pin no. 7 is grounded; the other pins represent inputs and outputs.

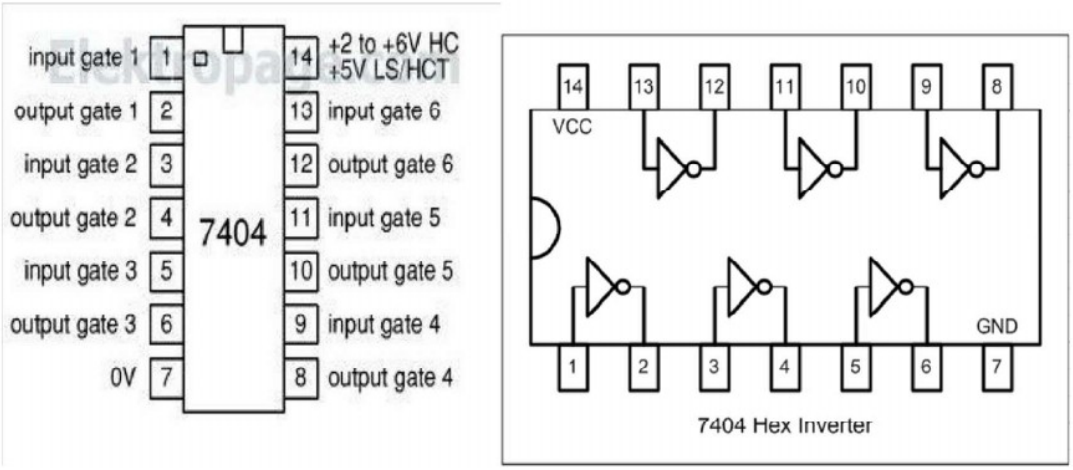


Fig.: Pin diagram of IC 7404 (Hex inverter)

IC 7408

This is an AND gate IC having fourteen pins. Power supply is given to pin no. 14 and pin no. 7 is grounded; the other pins represent inputs and outputs.

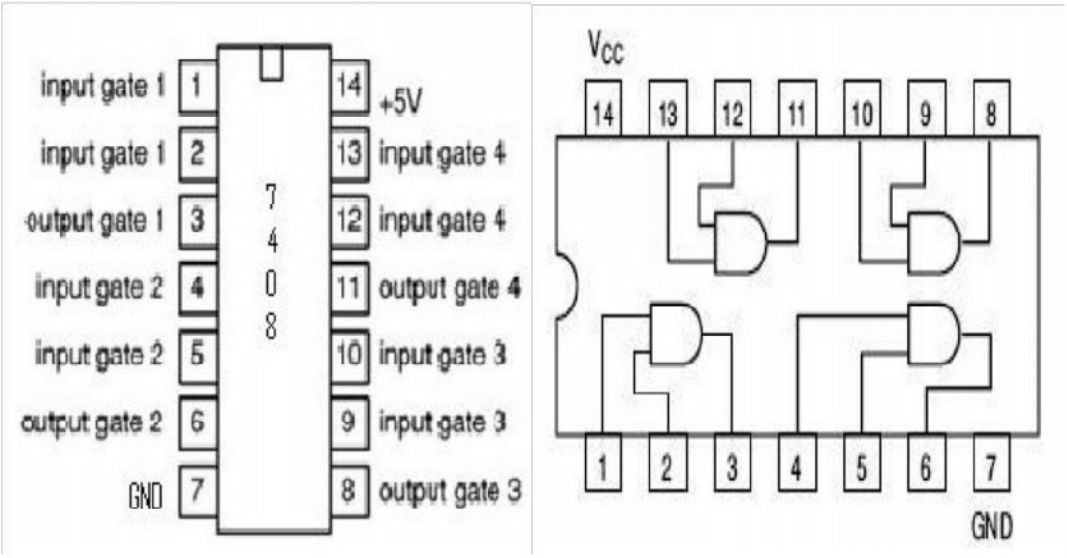


Fig.: Pin diagram of IC 7408 (Quad 2-input AND gate)

IC 7432

This is an OR gate IC having fourteen pins. Power supply is given to pin no. 14 and pin no. 7 is grounded; the other pins represent inputs and outputs.

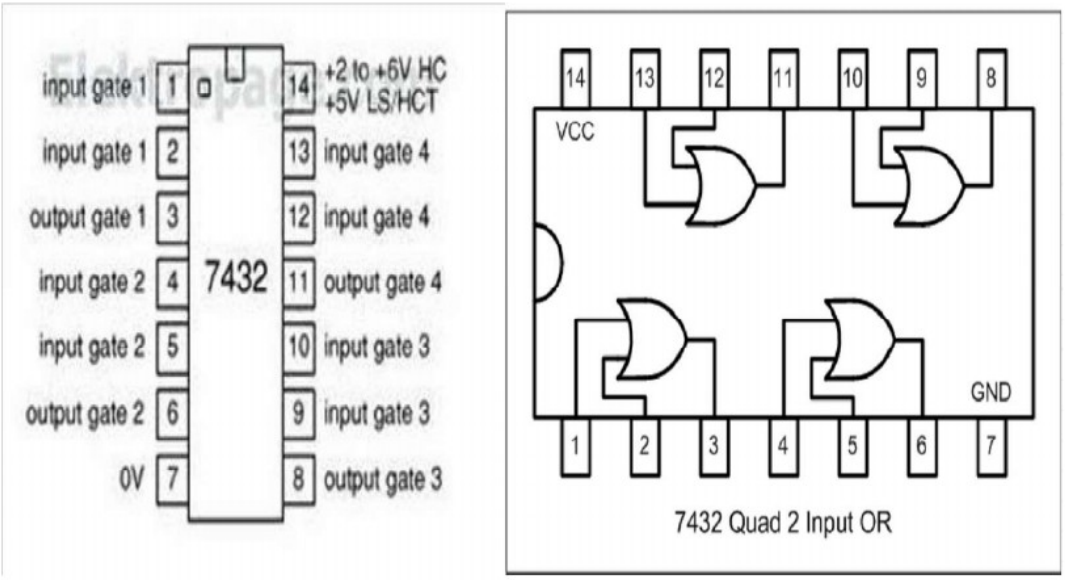


Fig.: Pin diagram of IC 7432 (Quad 2-input OR gate)

IC 7486

This is an EX-OR gate IC having fourteen pins. Power supply is given to pin no. 14 and pin no. 7 is grounded; the other pins represent inputs and outputs.

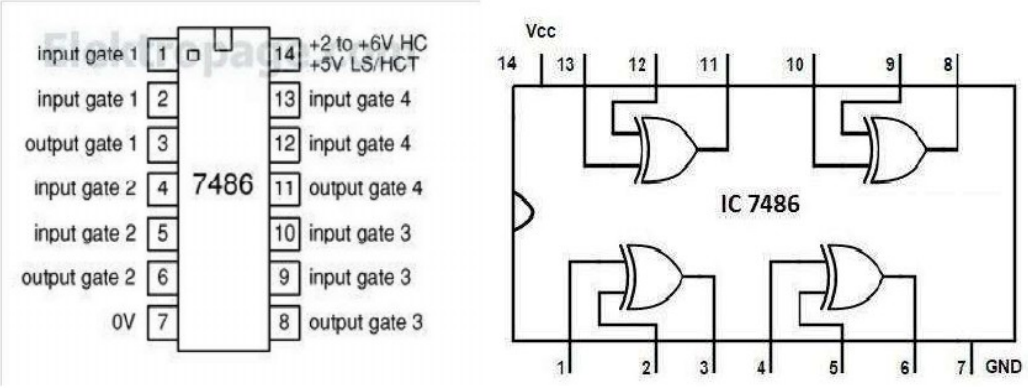


Fig.: Pin diagram of IC 7486 (Quad 2-input EX-OR gate)

Procedure

Identifying the pins of an IC

- Every IC has a notch.
- Place the IC in such a way that the notch remains on the left side.
- Then count the pins from left to right along the bottom row, then go to the opposite side and count from right to left.

IC 7400

- IC 7400 was fixed on the digital trainer kit.
- IC 7400 is a NAND gate IC. It has 14 pins.
- Power supply is given to pin no. 14 and pin no. 7 is ground.
- Pin no. 1 and pin no. 2 are inputs while pin no. 3 is the output.
- Pin no. 4 and pin no. 5 are inputs while pin no. 6 is the output.
- Pin no. 9 and pin no. 10 are inputs while pin no. 8 is the output.
- Pin no. 12 and pin no. 13 are inputs while pin no. 11 is the output.

IC 7402

- IC 7402 was fixed on the digital trainer kit.
- IC 7402 is a NOR gate IC. It has 14 pins.
- Power supply is given to pin no. 14 and pin no. 7 is ground.
- Pin no. 2 and pin no. 3 are inputs while pin no. 1 is the output.
- Pin no. 5 and pin no. 6 are inputs while pin no. 4 is the output.
- Pin no. 8 and pin no. 9 are inputs while pin no. 10 is the output.
- Pin no. 11 and pin no. 12 are inputs while pin no. 13 is the output.

IC 7404

- IC 7404 was fixed on the digital trainer kit.
- IC 7404 is a NOT gate IC. It has 14 pins.
- Power supply is given to pin no. 14 and pin no. 7 is ground.
- Pin no. 1 is the input while pin no. 2 is the output.
- Pin no. 3 is the input while pin no. 4 is the output.

- Pin no. 5 is the input while pin no. 6 is the output.
- Pin no. 9 is the input while pin no. 8 is the output.
- Pin no. 11 is the input while pin no. 10 is the output.
- Pin no. 13 is the input while pin no. 12 is the output.

IC 7408

- IC 7408 was fixed on the digital trainer kit.
- IC 7408 is an AND gate IC. It has 14 pins.
- Power supply is given to pin no. 14 and pin no. 7 is ground.
- Pin no. 1 and pin no. 2 are inputs while pin no. 3 is the output.
- Pin no. 4 and pin no. 5 are inputs while pin no. 6 is the output.
- Pin no. 9 and pin no. 10 are inputs while pin no. 8 is the output.
- Pin no. 12 and pin no. 13 are inputs while pin no. 11 is the output.

IC 7432

- IC 7432 was fixed on the digital trainer kit.
- IC 7432 is an OR gate IC. It has 14 pins.
- Power supply is given to pin no. 14 and pin no. 7 is ground.
- Pin no. 1 and pin no. 2 are inputs while pin no. 3 is the output.
- Pin no. 4 and pin no. 5 are inputs while pin no. 6 is the output.
- Pin no. 9 and pin no. 10 are inputs while pin no. 8 is the output.
- Pin no. 12 and pin no. 13 are inputs while pin no. 11 is the output.

IC 7486

- IC 7486 was fixed on the digital trainer kit.
- IC 7486 is an EX-OR gate IC. It has 14 pins.
- Power supply is given to pin no. 14 and pin no. 7 is ground.
- Pin no. 1 and pin no. 2 are inputs while pin no. 3 is the output.
- Pin no. 4 and pin no. 5 are inputs while pin no. 6 is the output.
- Pin no. 9 and pin no. 10 are inputs while pin no. 8 is the output.
- Pin no. 12 and pin no. 13 are inputs while pin no. 11 is the output.

Conclusion

From the above experiment, we have studied different digital ICs.

EXPERIMENT NO. 02

Aim

To verify the truth tables of NOT, AND, OR, NOR, NAND, XOR and XNOR gates using ICs, and simplification of Boolean expressions.

Apparatus Required

- Digital logic trainer kit
- Connecting probes
- AC supply (220 V)
- ICs (7400, 7402, 7404, 7408, 7432, 7486)

1. NOT Gate

Theory

1. The NOT gate is also called an inverter.
2. It is one of the basic logic gates.
3. It has one input and one output.

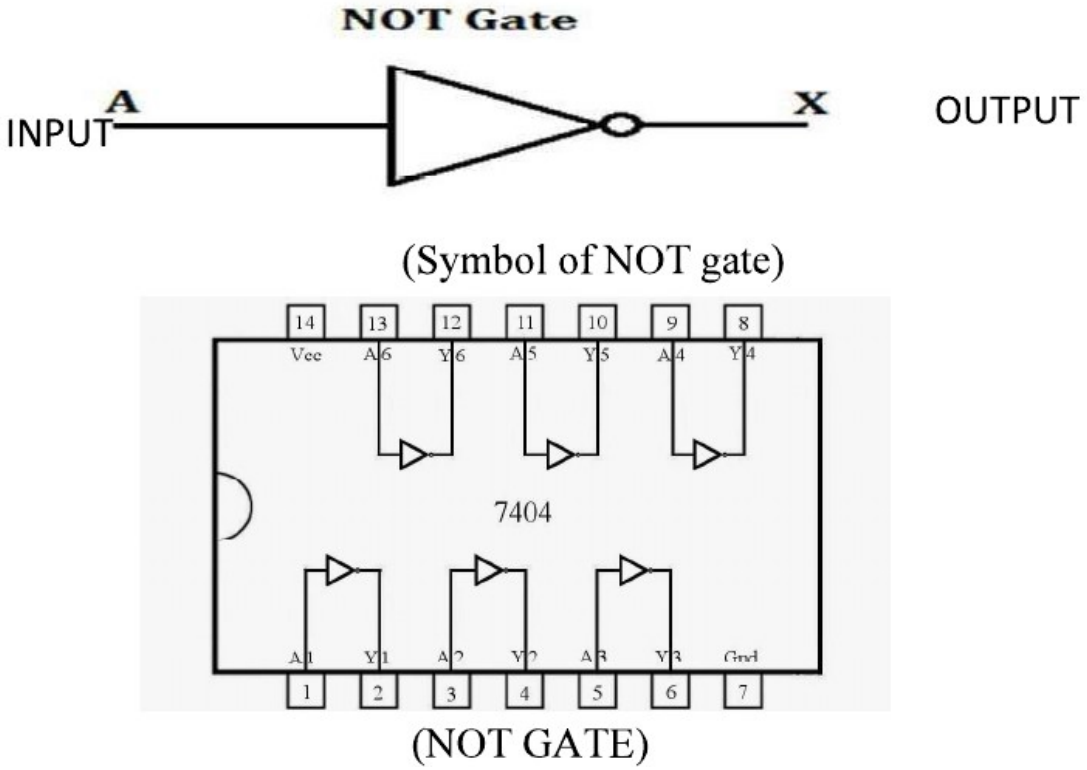


Fig.: Symbol of NOT gate and IC 7404

Truth Table

Input (A)	Output (Ā)
0	1
1	0

- When 0 was given as input, the output obtained was 1.
- When 1 was given as input, the output obtained was 0.

Procedure

1. Connect the input logic switches and the output LED indicator using connecting probes as per the logic circuit diagram on the trainer kit.
2. Give the various combinations of inputs and observe the output.
3. Tally the result with the truth table.

- IC 7404 was fixed on the breadboard of the digital trainer kit.
- Power supply is given to pin no. 14 and pin no. 7 was connected to ground.
- Input was given to pin no. 1.
- Output was taken from pin no. 2.

2. AND Gate

Theory

1. The AND gate is one of the basic logic gates.
2. It has two inputs and only one output.

Truth Table

A	B	Output (A·B)
0	0	0
0	1	0
1	0	0
1	1	1

- When 0 and 0 were given as input, the output obtained was 0.
- When 0 and 1 were given as input, the output obtained was 0.
- When 1 and 0 were given as input, the output obtained was 0.
- When 1 and 1 were given as input, the output obtained was 1.

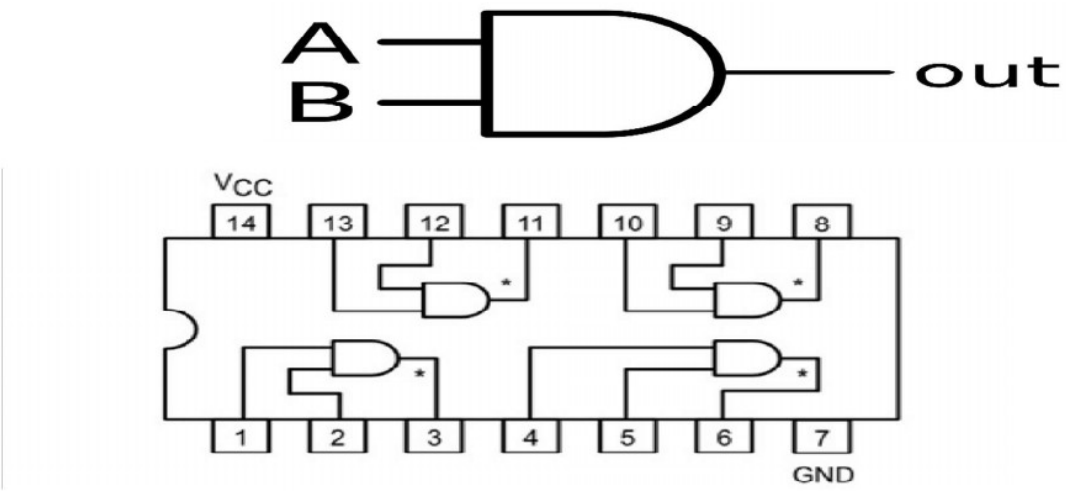


Fig.: Symbol of AND gate and IC 7408

Procedure

1. Connect the input logic switches and the output LED indicator using connecting probes as per the logic diagram on the trainer kit.
2. Give the various combinations of inputs and observe the output.
3. Tally the result with the truth table.

- IC 7408 was fixed on the breadboard of the digital trainer kit.
- Power supply is given to pin no. 14 and pin no. 7 was connected to ground.
- Input was given to pin no. 1 and pin no. 2.
- Output was taken from pin no. 3.

3. OR Gate

Theory

- The OR gate is one of the basic logic gates.
- It has two inputs and only one output.

Truth Table

A	B	Output (A + B)
0	0	0
0	1	1
1	0	1
1	1	1

- When 0 and 0 were given as input, the output obtained was 0.
- When 0 and 1 were given as input, the output obtained was 1.
- When 1 and 0 were given as input, the output obtained was 1.
- When 1 and 1 were given as input, the output obtained was 1.

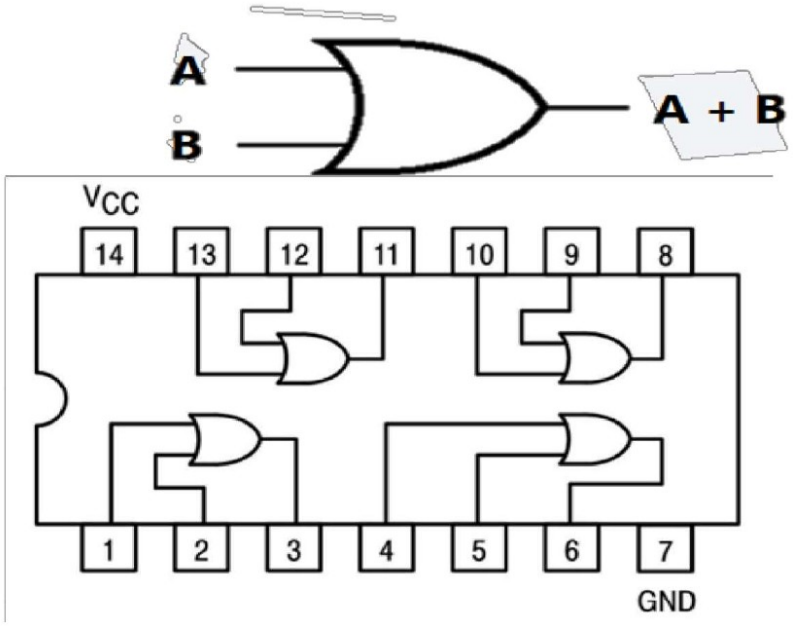


Fig.: Symbol of OR gate and IC 7432

Procedure

1. Connect the input logic switches and the output LED indicator using connecting probes as per the logic circuit diagram on the trainer kit.
2. Give the various combinations of inputs and observe the output.
3. Tally the result with the truth table.

- IC 7432 was fixed on the breadboard of the digital trainer kit.
- Power supply is given to pin no. 14 and pin no. 7 was connected to ground.
- Input was given to pin no. 1 and pin no. 2. Output was taken from pin no. 3.

4. NAND Gate

Theory

1. NAND is the complement of the AND gate.
2. It has two inputs and only one output.

Truth Table

A	B	A·B	Output (A·B)′
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

- When 0 and 0 were given as input, the output obtained was 1.
- When 0 and 1 were given as input, the output obtained was 1.
- When 1 and 0 were given as input, the output obtained was 1.

- When 1 and 1 were given as input, the output obtained was 0.

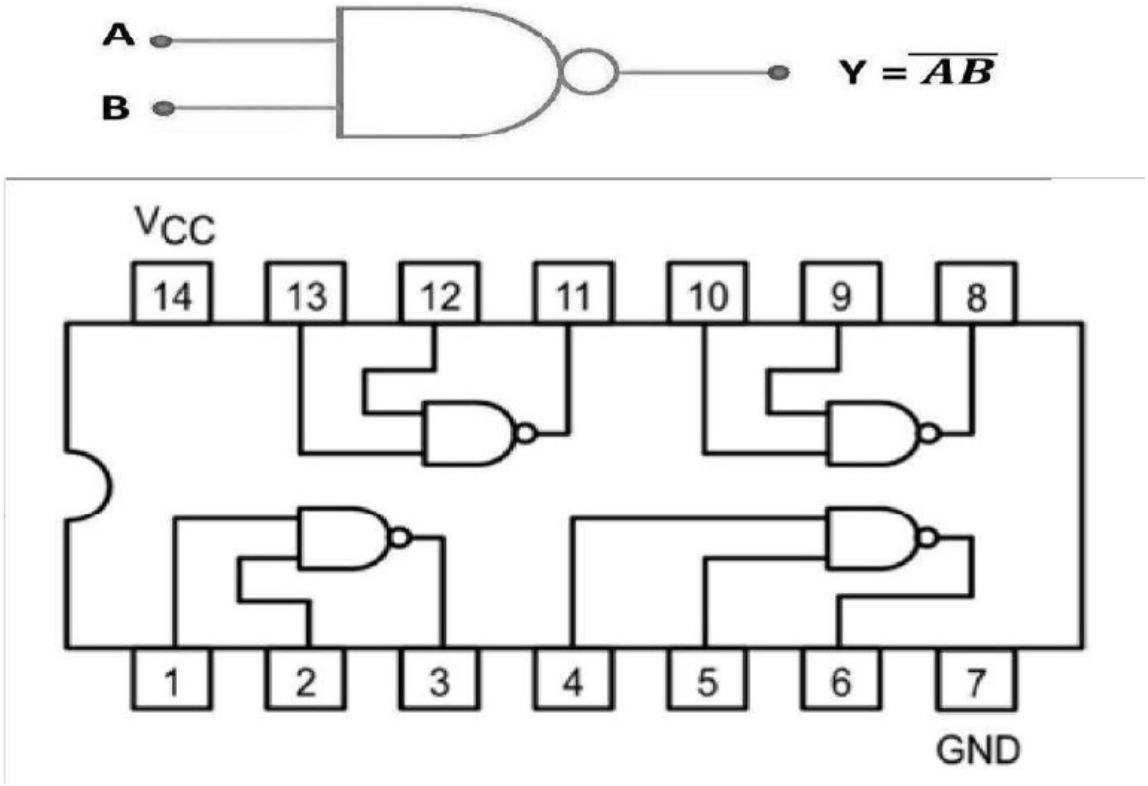


Fig.: Symbol of NAND gate and IC 7400

Procedure

1. Connect the input logic switches and the output LED indicator using connecting probes as per the logic circuit diagram on the trainer kit.
2. Give the various combinations of inputs and observe the output.
3. Tally the result with the truth table.

- IC 7400 was fixed on the breadboard of the digital trainer kit.
- Power supply is given to pin no. 14 and pin no. 7 was connected to ground.
- Input was given to pin no. 1 and pin no. 2. Output was taken from pin no. 3.

5. NOR Gate

Theory

1. The NOR gate is the complement of the OR gate.
2. It has two inputs and only one output.

Truth Table

A	B	Output (A + B)′
0	0	1
0	1	0
1	0	0

A	B	Output (A + B)′
1	1	0

- When 0 and 0 were given as input, the output obtained was 1.
- When 0 and 1 were given as input, the output obtained was 0.
- When 1 and 0 were given as input, the output obtained was 0.
- When 1 and 1 were given as input, the output obtained was 0.

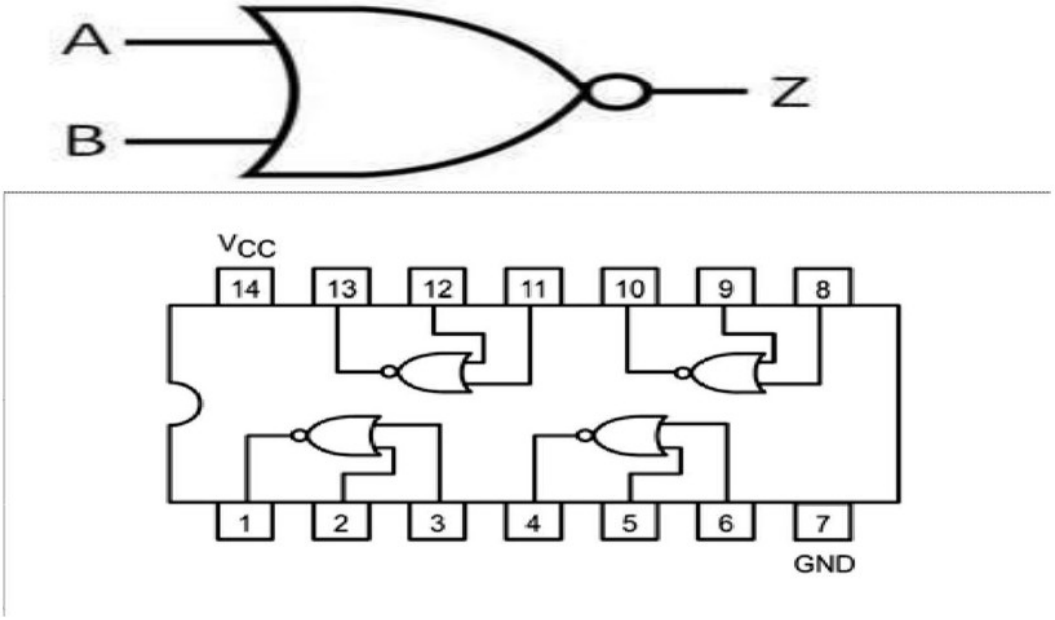


Fig.: Symbol of NOR gate and IC 7402

Procedure

1. Connect the input logic switches and the output LED indicator using connecting probes as per the logic circuit diagram on the trainer kit.
2. Give the various combinations of inputs and observe the output.
3. Tally the result with the truth table.

- IC 7402 was fixed on the breadboard of the digital trainer kit.
- Power supply is given to pin no. 14 and pin no. 7 was connected to ground.
- Input was given to pin no. 2 and pin no. 3. Output was taken from pin no. 1.

6. EX-OR Gate

Theory

1. It has two inputs and only one output.
2. The EX-OR output is high only when an odd number of inputs is high.

Truth Table

A	B	Output (A ⊕ B)
0	0	0
0	1	1
1	0	1
1	1	0

- When 0 and 0 were given as input, the output obtained was 0.
- When 0 and 1 were given as input, the output obtained was 1.
- When 1 and 0 were given as input, the output obtained was 1.
- When 1 and 1 were given as input, the output obtained was 0.

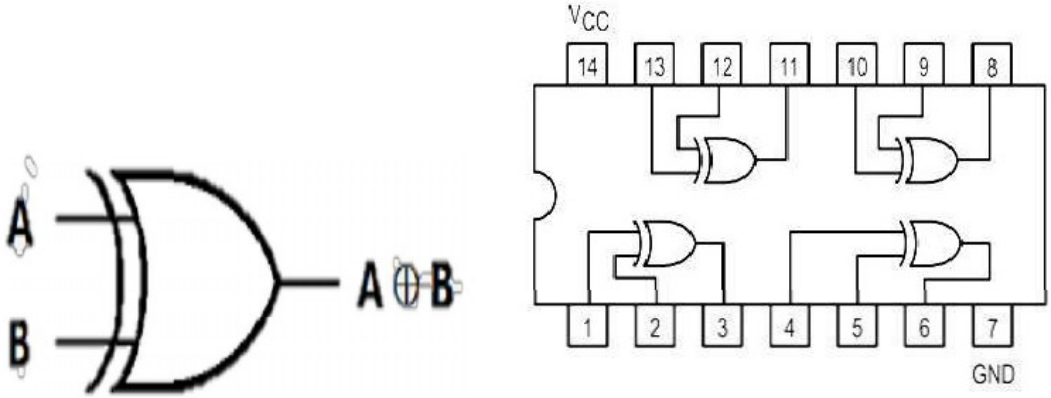


Fig.: Symbol of EX-OR gate and IC 7486

Procedure

1. Connect the input logic switches and the output LED indicator using connecting probes as per the logic circuit diagram on the trainer kit.
2. Give the various combinations of inputs and observe the output.
3. Tally the result with the truth table.

- IC 7486 was fixed on the breadboard of the digital trainer kit.
- Power supply is given to pin no. 14 and pin no. 7 was connected to ground.
- Input was given to pin no. 1 and pin no. 2. Output was taken from pin no. 3.

7. EX-NOR Gate (using IC 7486 and IC 7404)

Truth Table

A	B	Output Y = (A ⊕ B)′
0	0	1
0	1	0
1	0	0

A	B	Output Y = (A ⊕ B)′
1	1	1

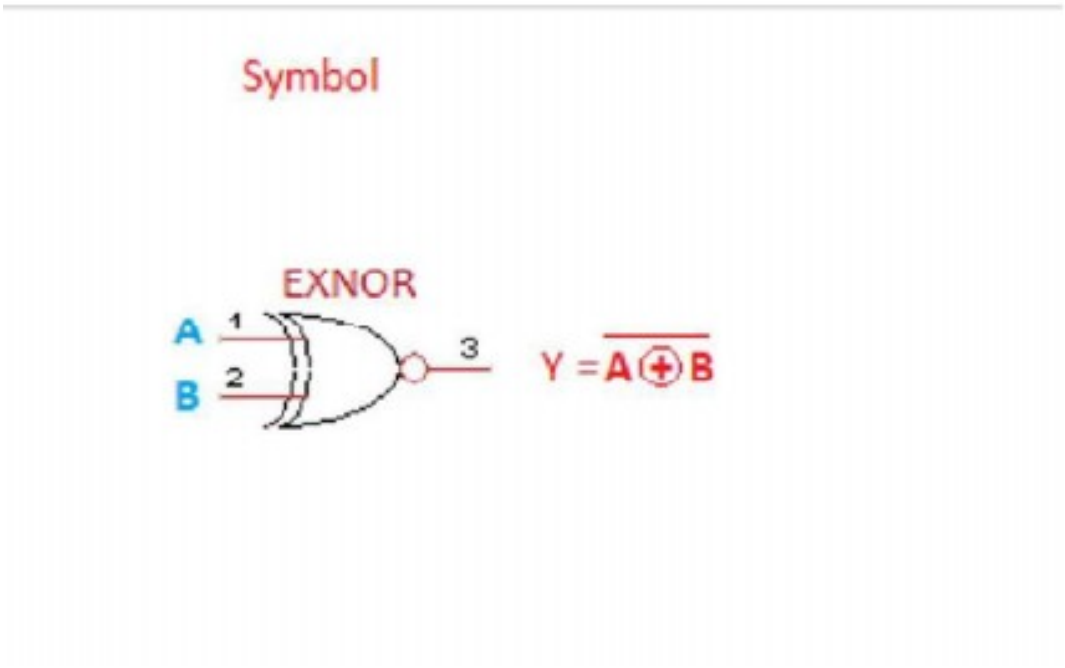


Fig.: Symbol of EX-NOR gate

- When 0 and 0 were given as input, the output obtained was 1.
- When 0 and 1 were given as input, the output obtained was 0.
- When 1 and 0 were given as input, the output obtained was 0.
- When 1 and 1 were given as input, the output obtained was 1.

Procedure

- IC 7486 and IC 7404 were fixed on the breadboard of the digital trainer kit.
- Power supply is given to pin no. 14 and pin no. 7 was connected to ground in both the ICs.
- Input was given to pin no. 1 and pin no. 2 of IC 7486.
- Output was taken from pin no. 3 of IC 7486.
- The output of IC 7486 was given to pin no. 1 of IC 7404 (NOT gate).
- The final output was taken from pin no. 2 of IC 7404.

Conclusion

From the above experiment, we have verified the truth tables of various logic gates.

EXPERIMENT NO. 03

Aim of the Experiment

To construct and verify the operation of a half adder and a full adder using basic gates.

Apparatus Required

- Digital logic trainer kit
- Connecting probes
- AC supply (220 V)
- AND, OR and EX-OR gates – IC 7408, 7432 and 7486 respectively
- Patch cords

Theory

An adder is a combinational logic circuit that can add two or more binary bits, resulting in a sum and a carry bit. It is of two types:

1. Half Adder
2. Full Adder

1. Half Adder

A half adder is a combinational logic circuit that adds two binary bits. Let the inputs to the circuit be A and B, and the outputs be Sum (S) and Carry (C).

$$Sum = A \oplus B = A\bar{B} + \bar{A}B$$

$$Carry = AB$$



Fig.: Block diagram of half adder

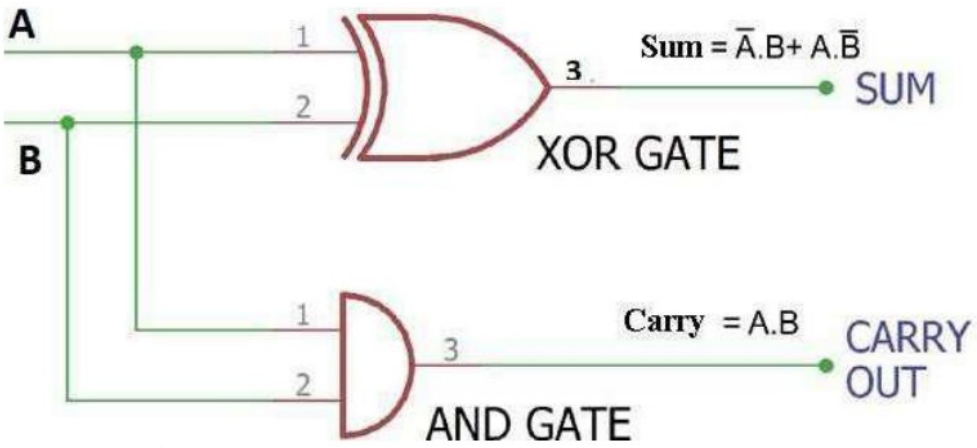


Fig.: Logic circuit of half adder

Truth Table (Half Adder)

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Procedure (Half Adder)

1. Fix IC 7486 and IC 7408 on the trainer board.
2. Connect pins 1 and 2 of IC 7486 as inputs.
3. Connect pin 3 of IC 7486 to the output where the sum is to be verified.
4. Pin 1 of IC 7408 is shorted with pin 1 of IC 7486. Similarly, pin 2 of IC 7408 is shorted with pin 2 of IC 7486.
5. Pin 3 of IC 7408 was connected to the output where the carry is to be verified.
6. The ground and supply pins of all the ICs, i.e. pin no. 7 and 14, are shorted with each other.
7. Then switch ON the power supply of the trainer kit.

2. Full Adder

- It is a combinational logic circuit which adds two data bits along with the previous carry, resulting in sum and carry bits.
- Let A and B be the data bits and C be the carry.

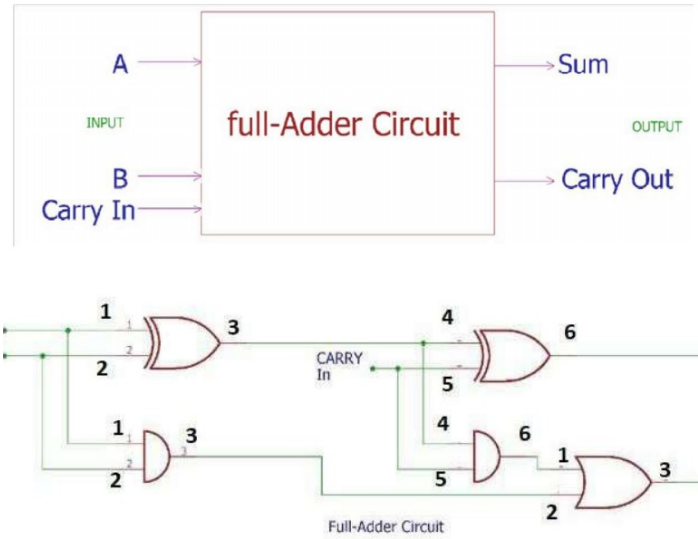


Fig.: Block diagram and logic circuit of full adder

Truth Table (Full Adder)

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Procedure (Full Adder)

- Fix IC 7432, 7486 and 7408 on the trainer board.
- The ground and supply pins of all the ICs, i.e. pin no. 7 and 14, are shorted with each other.
- Input was given to pin no. 1, pin no. 2 and pin no. 5 of IC 7486.
- Pin no. 1 and 2 of IC 7486 are shorted with pin no. 1 and 2 of IC 7408.
- Short pin no. 3 of IC 7486 to pin no. 4 of IC 7486.
- Pin no. 3 of IC 7408 is shorted with pin no. 2 of IC 7432, and pin no. 4 of IC 7408 is shorted with pin no. 4 of IC 7486.
- Short pin no. 5 of IC 7408 to pin no. 5 of IC 7486.
- Short pin no. 6 of IC 7408 with pin no. 1 of IC 7432.
- Observe the output for sum from pin no. 6 of IC 7486.
- Observe the output for carry from pin no. 3 of IC 7432.

- Then switch ON the power supply of the trainer board.

Conclusion

From the above experiment, we successfully implemented the half adder and full adder using logic gates.

EXPERIMENT NO. 04

Aim of the Experiment

To implement a half subtractor and a full subtractor using logic circuits.

Apparatus Required

- Digital logic trainer kit
- Connecting probes
- AC supply (220 V)

Theory

- A subtractor is a combinational logic circuit that can subtract two or three binary data bits, resulting in a difference and a borrow.
- It is of two types: half subtractor and full subtractor.

Half Subtractor

A half subtractor is a combinational logic circuit that subtracts 2 bits and produces their difference and borrow.

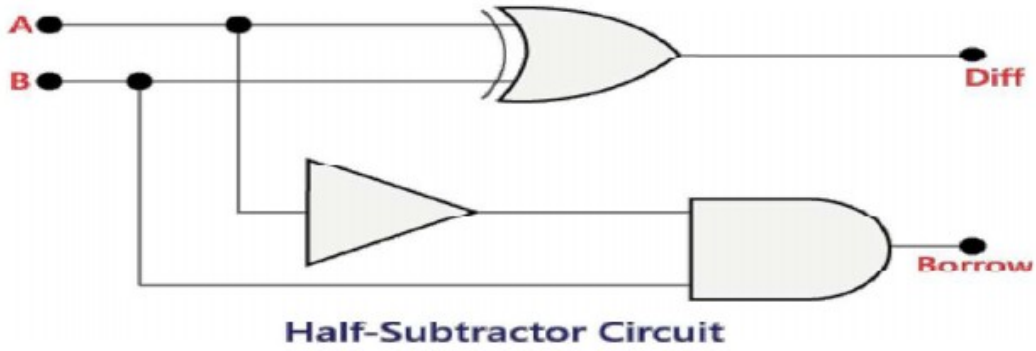


Fig.: Half subtractor circuit

Truth Table (Half Subtractor)

A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

$$Difference = \bar{A}B + A\bar{B} = A \oplus B$$

$$Borrow = \bar{A}B$$

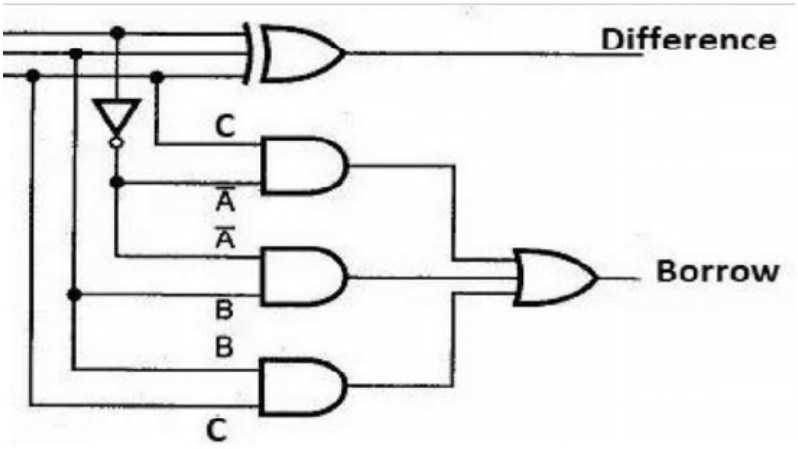
Procedure (Half Subtractor)

- Fix IC 7404, 7408 and 7486 on the trainer board.
- Connect pin numbers 1 and 2 of IC 7486 to the inputs of the trainer board.

- Connect pin number 3 of IC 7486 to the output on the trainer board where the difference is verified with the truth table.
- Pin number 1 of IC 7486 is shorted with pin number 1 of IC 7404.
- Pin number 2 of IC 7486 is shorted with pin no. 2 of IC 7408. Pin number 2 of IC 7404 is shorted with pin number 1 of IC 7408.
- Pin number 3 of IC 7408 is connected to the output of the trainer board where the borrow is verified from the truth table.

Full Subtractor

A full subtractor is a combinational logic circuit that performs subtraction involving 3 bits, namely the minuend bit, the subtrahend bit and the borrow from the previous stage.



(FULL SUBSTRACTOR CIRCUIT)

Fig.: Full subtractor circuit

Truth Table (Full Subtractor)

A	B	Bin	Difference (D)	Borrow (Bo)
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Procedure (Full Subtractor)

- Fix IC 7408, 7486, 7432 and 7404 on the trainer board. Connect pin number 7 to ground and pin number 14 to the supply of each IC.

- Pin numbers 1, 4, 5 of IC 7486 are given inputs from the trainer board. Pin number 1 of IC 7486 is shorted with pin number 5 of IC 7408.
- Pin numbers 2, 6 of IC 7486 are shorted with pin no. 3 of IC 7404.
- Pin numbers 4 and 5 of IC 7486 are shorted with pin no. 1 of IC 7404 and pin no. 2 of IC 7408. Pin no. 2 of IC 7404 is also connected to pin no. 1 of IC 7408 as input.
- Pin no. 3 of IC 7408 is shorted with pin no. 2 of IC 7432.
- Pin no. 4 of IC 7404 is connected to pin no. 4 of IC 7408 as input.
- Pin no. 6 of IC 7408 is shorted with pin no. 1 of IC 7432 as input.
- Pin number 3 of IC 7486 is connected to the output of the trainer board, where the difference is verified with the truth table.
- Pin number 3 of IC 7432 is connected to the output of the trainer board, where the borrow is verified with the truth table.

Conclusion

From the above experiment, we have implemented the half and full subtractor using logic gates.

EXPERIMENT NO. 05

Aim of the Experiment

To design and implement a 4-bit binary to Gray code converter.

Theory

Binary to Gray Code Converter

The binary to Gray code converter is a logic circuit used to convert a binary number into its equivalent Gray code. By putting a 0 as the MSB above the axis and a 1 as the MSB below the axis, and reflecting the (n − 1) bit code about an axis after 2^{n-1} rows, we can obtain the n-bit Gray code.

How to Convert Binary to Gray Code

- In the Gray code, the MSB will always be the same as the first bit of the given binary number.
- To get the 2nd bit of the Gray code, we perform the exclusive-OR (XOR) of the 1st and 2nd bits of the binary number. If both are different the result will be 1, else the result will be 0.
- To get the 3rd bit of the Gray code, we perform the XOR of the 2nd and 3rd bits of the binary number. The process remains the same for the 4th bit of the Gray code.
- The bits of the 4-bit Gray code are considered as G4, G3, G2 and G1.

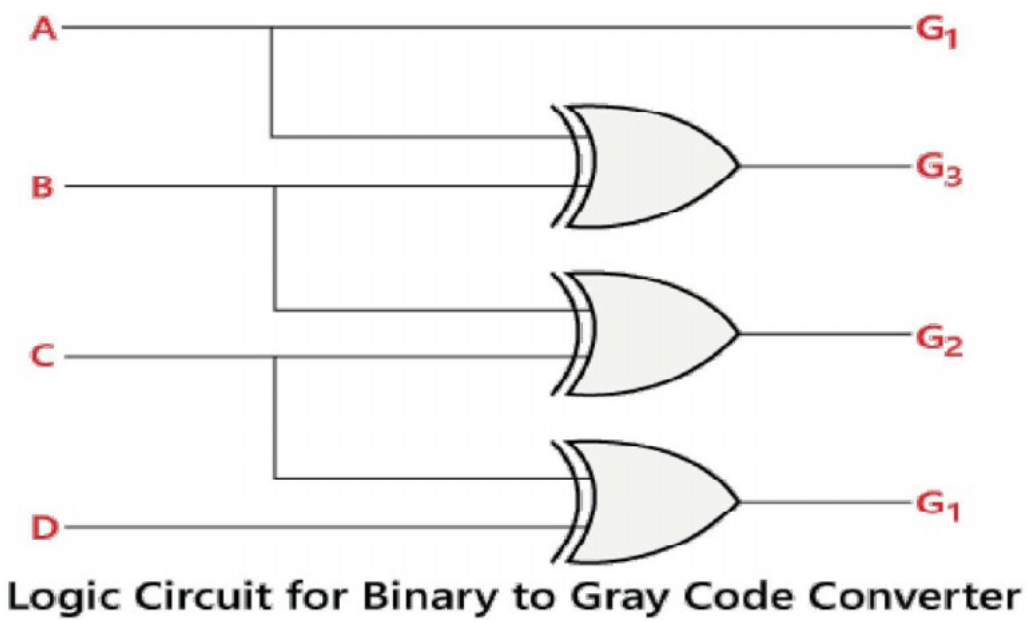


Fig.: Logic circuit for binary to Gray code converter

4-bit Binary to Gray Code Conversion Table

Decimal Number	4-bit Binary Number	4-bit Gray Code
0	0000	0000
1	0001	0001

Decimal Number	4-bit Binary Number	4-bit Gray Code
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

Procedure

- Connect A, B, C and D to the logic inputs (low or high).
- The outputs G1, G2, G3 and G4 are connected to the logic LED indicators.
- Now give inputs using the toggle switches available on the digital IC trainer.
- Verify the truth table for binary to Gray conversion.

Conclusion

From the above experiment, we successfully studied the design of a binary to Gray code converter.

EXPERIMENT NO. 06

Aim of the Experiment

To design and implement a 1-bit / 2-bit magnitude comparator.

Apparatus Required

- Magnitude comparator trainer kit
- Connecting wires

Theory

- A comparator is a logic circuit used to compare the magnitude of two binary numbers.
- The EX-NOR gate is a basic comparator because its output is 1 only if its two input bits are equal.
- Let two binary numbers be A and B. The two binary numbers will be equal only when each bit is equal, i.e. A = B.
- If A = 0, B = 0, then A = B.
- If A = 0, B = 1, then A < B.
- If A = 1, B = 0, then A > B.
- If A = 1, B = 1, then A = B.

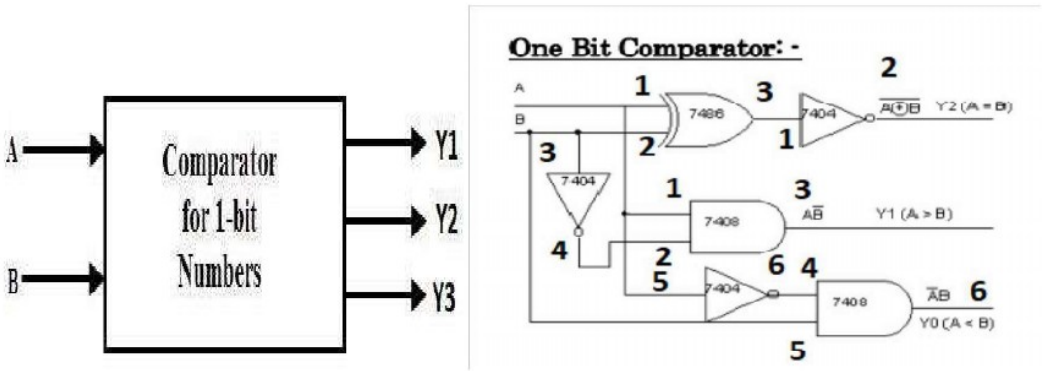


Fig.: Block diagram and logic circuit of 1-bit comparator

Truth Table (1-bit Comparator)

A	B	Y1 (A > B)	Y2 (A = B)	Y3 (A < B)
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

Magnitude Comparator

A digital magnitude comparator is a combinational circuit that compares 2 binary numbers (consider A and B) and determines their magnitude, in order to find out whether one number is equal to, less than or greater than the other binary number.

A 2-bit comparator compares two binary numbers of 2 bits each and produces their relation, such as one number is equal to, greater than or less than the other number.

The first number is designated as A = A1A0 and the second number as B = B1B0. The comparator produces the outputs G = 1 if A > B, E = 1 if A = B, and L = 1 if A < B.

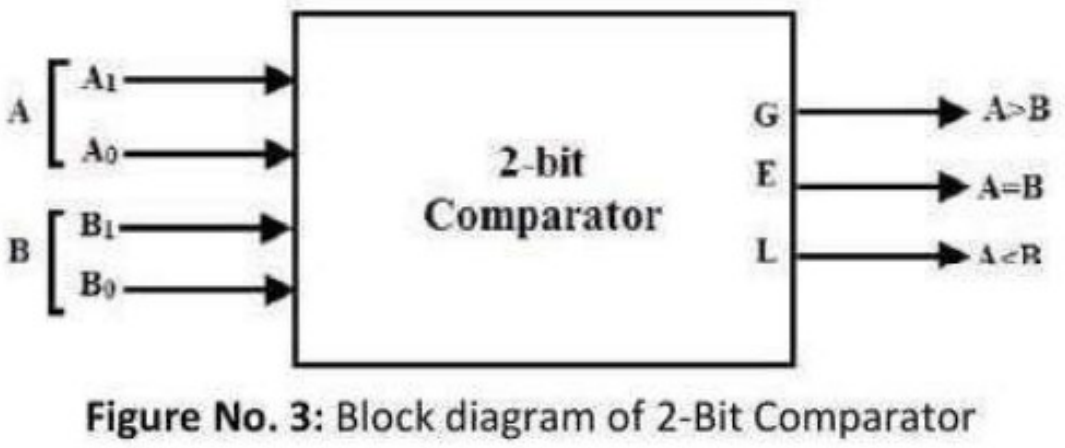


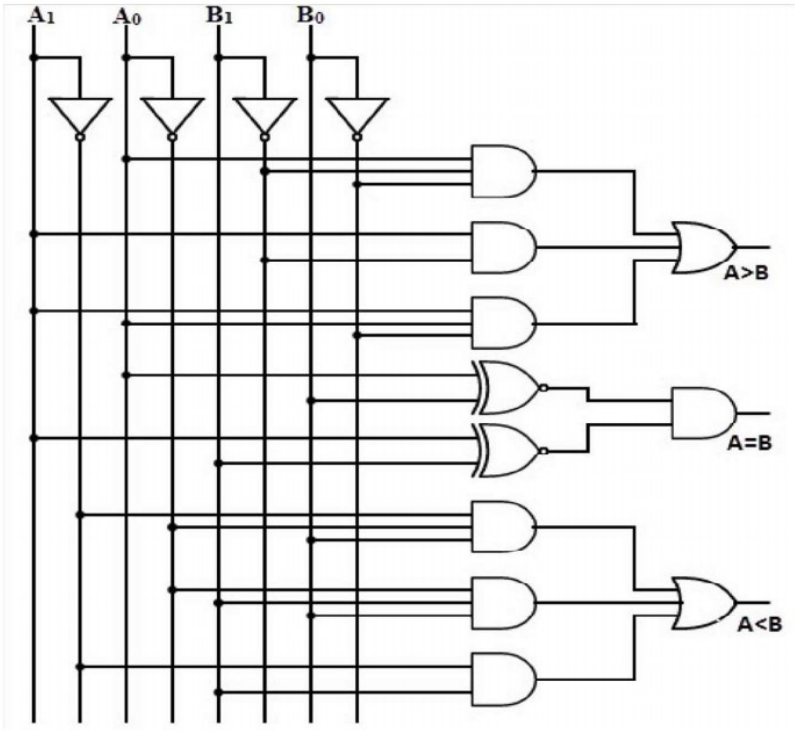
Figure No. 3: Block diagram of 2-Bit Comparator

Fig.: Block diagram of 2-bit comparator

Truth Table (2-bit Comparator)

A1	A0	B1	B0	A > B	A = B	A < B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0

A1	A0	B1	B0	A > B	A = B	A < B
1	1	1	0	1	0	0
1	1	1	1	0	1	0



(Logic circuit of 2 bit magnitude comparator)

Fig.: Logic circuit of 2-bit magnitude comparator

Procedure

1. Set IC 7408, 7486 and 7404 on the trainer board.
2. Connect pin numbers 1 and 2 of IC 7486 as inputs.
3. Short pin 1 of IC 7486, pin no. 1 of IC 7408 and pin no. 5 of IC 7404.
4. Short pin number 3 of IC 7486 to pin no. 1 of IC 7404 as input, and take the output through pin number 2 of IC 7404.
5. Short pin number 2 of IC 7486, pin no. 3 of IC 7404 and pin no. 5 of IC 7408.
6. Short pin no. 6 of IC 7404 to pin no. 4 of IC 7408, and take the output at pin number 6.
7. Short pin number 4 of IC 7404 to pin no. 2 of IC 7408, and take the output at pin no. 3 of IC 7408.
8. Give the power supply to pin number 14 and ground to pin number 7.
9. Switch ON the power supply.
10. Verify the truth table.

Conclusion

From the above experiment, we successfully studied and implemented the 2-bit magnitude comparator.

General Guidelines and Safety Instructions

1. Sign in the log register as soon as you enter the lab and strictly observe your lab timings.
2. Strictly follow the written and verbal instructions given by the teacher / lab instructor. If you do not understand the instructions, the handouts and the procedures, ask the instructor or teacher.
3. It is mandatory to come to the lab in formal dress and wear your ID card.
4. Do not wear loose-fitting clothing or jewellery in the lab. Rings and necklaces are usually excellent conductors of electricity.
5. Mobile phones should be switched off in the lab. Keep bags in the bag rack.
6. Keep the labs clean at all times; no food and drinks are allowed inside the lab.
7. Intentional misconduct will lead to expulsion from the lab.
8. Do not insert connectors forcefully into the sockets.
9. NEVER try to experiment with the power from the wall plug.
10. Immediately report dangerous or exceptional conditions to the lab instructor / teacher: equipment that is not working as expected, wires or connectors that are broken, or equipment that smells or "smokes". If you are not sure what the problem is or what is going on, switch off the emergency shutdown.
11. Never use damaged instruments, wires or connectors. Hand over these parts to the lab instructor / teacher.
12. Be sure of the location of fire extinguishers and first aid kits in the laboratory.
13. After verification of the program output, turn off the power supply to the trainer kit. Do not take any item from the lab without permission.
14. The observation book and lab record should be carried to each lab. Programs of the current lab session are to be written in the observation book, and those of the previous lab session should be written in the lab record book. Both books should be corrected by the faculty in each lab.
15. Handling of the microprocessor trainer kit: Sensitive electronic circuits and electronic components have to be handled with great care. Inappropriate handling of electronic components can damage or destroy the devices. Therefore, always handle the electronic devices as indicated by the handout, the specifications in the data sheet or other documentation.

Steps to Execute the Program on 8085 Microprocessor Kit

Follow the steps given below in order to execute the program on the 8085 microprocessor kit:

1. Enter program
2. Enter data
3. Execute program
4. Check result

Execution Procedure

Assembly language programs for the 8085 microprocessor can be executed on its trainer kit as per the following steps.

Step 1: Storage of program machine codes. The machine codes of the program to be executed should be stored in the memory available on the 8085 trainer kit as:

RESET → EXAM MEM → Starting address of program (2000) → NEXT

Now enter all the machine codes, one after the other, followed by the key 'NEXT'.

Step 2: Declaration of inputs. Input values to the program should be declared as:

RESET → EXAM MEM → Input address → NEXT

Now enter all the input values, each followed by the key 'NEXT'.

Step 3: Execution of program. The program can be executed as:

RESET → GO → Starting address of program (2000) → EXEC

Step 4: Verification of output. The output of the executed program can be verified as:

RESET → EXAM MEM → Output address → NEXT

EXPERIMENT NO. 07

Aim of the Experiment

Write an assembly language program in the 8085 microprocessor for:

- (a) Addition of two 8-bit numbers, where the sum is 8/16 bit.
- (b) Subtraction of two 8-bit numbers, where the result is 8 bit.
- (c) Multiplication of two 8-bit numbers, where the result is 8/16 bit.
- (d) Division of two 8-bit numbers, where the result is 8 bit.

Apparatus Required

8085 microprocessor kit, +5 V power supply, keyboard.

Theory

(a) Addition of two 8-bit numbers (sum is 8/16 bit): The first number 98H is stored in memory location 2501H and the second number 9AH is stored in memory location 2502H. The result after addition will be stored in memory locations 2503H and 2504H. Consider that the program is written from memory location 2000H.

(b) Subtraction of two 8-bit numbers (result is 8 bit): The first number 49H is stored in memory location 2501H and the second number 32H is stored in memory location 2502H. The result after subtraction will be stored in memory location 2503H. Consider that the program is written from memory location 2000H.

(c) Multiplication of two 8-bit numbers (result is 8/16 bit): The HL register pair is first initialized to the address of the memory location at which the data is present. The data is brought to accumulator A, the other number from M is added, and the result is stored in the accumulator. The result is again stored into memory from the accumulator. The ADD instruction sets and clears flags according to the result.

(d) Division of two 8-bit numbers (result is 8 bit): The HL register pair is first initialized to the address of the memory location at which the data is present. The data is brought to accumulator A, the other number from M is added, and the result is stored in the accumulator. The result is again stored into memory from the accumulator. The ADD instruction sets and clears flags according to the result.

Algorithm

(a) Addition of two 8-bit numbers

- Start the program by loading the first data into the accumulator.
- Add the first number with the 2nd number directly from the memory location.
- Check for carry.
- Store the value of sum and carry in memory locations.
- Terminate the program.

(b) Subtraction of two 8-bit numbers

- Start the program by loading the first data into the accumulator.

- Subtract the 2nd number from the 1st number directly from the memory location.
- Store the difference value (present in the accumulator) to a memory location.
- Terminate the program.

(c) Multiplication of two 8-bit numbers

- Load the opcode in the specified address.
- Enter the data needed for execution of the program at the specified memory address.
- Execute the program and check the result at the given address.
- Change the data and execute the program each time, and check the result.

Program

(a) Addition of two 8-bit numbers (sum is 8/16 bit)

Memory Address	Machine Code	Label	Opcode	Operand	Comments
2000	21, 01, 25		LXI	H, 2501H	Address of 1st number in H-L pair
2003	0E, 00		MVI	C, 00	MSBs of sum in register C
2005	7E		MOV	A, M	1st number in accumulator
2006	23		INX	H	Address of 2nd number 2502 in H-L pair
2007	86		ADD	M	1st number + 2nd number
2008	D2, 0C, 20		JNC	AHEAD	Is carry? No, go to label AHEAD
200B	0C		INR	C	Yes, increment C
200C	32, 03, 25	AHEAD	STA	2503H	LSBs of sum in 2503H
200F	79		MOV	A, C	MSBs of sum in accumulator
2010	32, 04, 25		STA	2504H	MSBs of sum in 2504H
2013	76		HLT		Halt

(b) Subtraction of two 8-bit numbers (result is 8 bit)

Memory Address	Machine Code	Label	Opcode	Operand	Comments
2000	21, 01, 25		LXI	H, 2501H	Address of 1st number in H-L pair
2003	7E		MOV	A, M	1st number in accumulator
2004	23		INX	H	Address of 2nd number 2502 in

Memory Address	Machine Code	Label	Opcode	Operand	Comments
					H-L pair
2005	96		SUB	M	1st number − 2nd number
2006	23		INX	H	Content of H-L pair becomes 2503H
2007	77		MOV	M, A	Store result in 2503H
2008	76		HLT		Halt

(c) Multiplication of two 8-bit numbers (result is 8/16 bit)

Memory Address	Opcode	Mnemonics	Operand	Description
8000	21	LXI	H, 8250	Load 8-bit data from memory location 8250
8001	50			
8002	82			
8003	4E	MOV	C, M	Move 8-bit data from memory to register C
8004	3E	MVI	A, 00	Initialize accumulator to 00
8005	00			
8006	23	INX	H	Increment address of HL pair by 1
8007	86	ADD	M	Add content of accumulator with data stored in given memory location
8008	0D	DCR	C	Decrement counter by 1
8009	C2	JNZ	8007	Jump to given memory location and add the content again
800A	07			
800B	80			
800C	32	STA	9250	Store the result from accumulator to memory location 9250
800D	50			
800E	92			
800F	76	HLT		Stop the program

Observation

(a) Addition of two 8-bit numbers

	Set 1	**Set 2**
DATA 2501	98H	F5H
DATA 2502	9AH	8AH
RESULT 2503 (LSBs of sum)	32H	7FH
RESULT 2504 (MSBs of sum)	01H	01H

(b) Subtraction of two 8-bit numbers

	Set 1	**Set 2**
DATA 2501	49H	F8H
DATA 2502	32H	9BH
RESULT 2503	17H	5DH

(c) Multiplication of two 8-bit numbers

	Set 1	**Set 2**
DATA 8250		
DATA 8251		
RESULT 9250		

Conclusion

The program is executed and the results are stored in the memory locations.

EXPERIMENT NO. 08

Aim of the Experiment

Write an assembly language program in the 8085 microprocessor to find out:

- (a) 1's complement of an 8-bit number
- (b) 1's complement of a 16-bit number
- (c) 2's complement of an 8-bit number
- (d) 2's complement of a 16-bit number

Apparatus Required

8085 microprocessor kit, +5 V power supply, keyboard.

Theory

(a) 1's complement of an 8-bit number: The number 96H is placed in memory location 2501H. The result is stored in memory location 2502H. Consider that the program is written from memory location 2000H.

(b) 1's complement of a 16-bit number: The number 5485H is placed in memory locations 2501H and 2502H. The result is to be stored in memory locations 2503H and 2504H. Consider that the program is written from memory location 2000H.

(c) 2's complement of an 8-bit number: The number 96H is placed in memory location 2501H. The result is stored in memory location 2502H. Consider that the program is written from memory location 2000H.

(d) 2's complement of a 16-bit number: The number 5B8CH is placed in memory locations 2501H and 2502H. The result is to be stored in memory locations 2503H and 2504H. Consider that the program is written from memory location 2000H.

Algorithm

(a) 1's complement of an 8-bit number

- Start the program by loading the number into the accumulator.
- Take the complement of the accumulator.
- Store the accumulator content in a memory location. Terminate the program.

(b) 1's complement of a 16-bit number

- Start the program by loading the 8 LSBs of the number into the accumulator.
- Take the complement of the accumulator.
- Store the accumulator content in a memory location.
- Load the 8 MSBs of the number into the accumulator.
- Take the complement of the accumulator.
- Store the accumulator content in a memory location.
- Terminate the program.

(c) 2's complement of an 8-bit number

- Start the program by loading the number into the accumulator.
- Take the complement of the accumulator (1's complement).
- Increment the accumulator content (2's complement).
- Store the accumulator content in a memory location.
- Terminate the program.

(d) 2's complement of a 16-bit number

- Start the program by loading the 8 LSBs of the number into the accumulator.
- Take the complement of the accumulator (1's complement).
- Add 1 to the accumulator content (2's complement).
- Store the accumulator content in a memory location.
- Check for carry.
- Load the 8 MSBs of the number into the accumulator.
- Take the complement of the accumulator (1's complement).
- Add carry.
- Store the accumulator content in a memory location.
- Terminate the program.

Program

(a) 1's complement of an 8-bit number

Memory Address	Machine Code	Label	Opcode	Operand	Comments
2000	3A, 01, 25		LDA	2501H	Get data in accumulator
2003	2F		CMA		Take its complement
2004	32, 02, 25		STA	2502H	Store result in 2502H
2007	76		HLT		Halt

(b) 1's complement of a 16-bit number

Memory Address	Machine Code	Label	Opcode	Operand	Comments
2000	21, 01, 25		LXI	H, 2501H	Address of LSBs of the number
2003	7E		MOV	A, M	8 LSBs of the number in accumulator
2004	2F		CMA		Complement the 8 LSBs of the number
2005	32, 03, 25		STA	2503H	Store 8 LSBs of result

Memory Address	Machine Code	Label	Opcode	Operand	Comments
2008	23		INX	H	Address of 8 MSBs of the number
2009	7E		MOV	A, M	8 MSBs of the number in accumulator
200A	2F		CMA		Complement the 8 MSBs of the number
200B	32, 04, 25		STA	2504H	Store 8 MSBs of result
200E	76		HLT		Halt

(c) 2's complement of an 8-bit number

Memory Address	Machine Code	Label	Opcode	Operand	Comments
2000	3A, 01, 25		LDA	2501H	Get data in accumulator
2003	2F		CMA		Take its 1's complement
2004	3C		INR	A	Take 2's complement
2005	32, 02, 25		STA	2502H	Store result in 2502H
2008	76		HLT		Halt

(d) 2's complement of a 16-bit number

Memory Address	Machine Code	Label	Opcode	Operand	Comments
2000	21, 01, 25		LXI	H, 2501H	Address of 8 LSBs of the number
2003	06, 00		MVI	B, 00H	Use register B to store carry
2005	7E		MOV	A, M	8 LSBs in accumulator
2006	2F		CMA		1's complement of 8 LSBs of the number
2007	C6, 01		ADI	01	2's complement of 8 LSBs of the number
2009	32, 03, 25		STA	2503H	Store 8 LSBs of the result
200C	D2, 10, 20		JNC	GO	Is carry? No, go to label GO
200F	04		INR	B	Store carry
2010	23	GO	INX	H	Address of 8 MSBs of the number

Memory Address	Machine Code	Label	Opcode	Operand	Comments
2011	7E		MOV	A, M	8 MSBs in accumulator
2012	2F		CMA		1's complement of 8 MSBs of the number
2013	80		ADD	B	Add carry
2014	32, 04, 25		STA	2504H	Store 8 MSBs of the result
2017	76		HLT		Halt

Observation

(a) 1's complement of an 8-bit number

	Set 1	Set 2
DATA 2501	96H	E4H
RESULT 2502	69H	1BH

(b) 1's complement of a 16-bit number

	Set 1	Set 2
DATA 2501	85H	7EH
DATA 2502	54H	89H
RESULT 2503	7AH	81H
RESULT 2504	ABH	76H

(c) 2's complement of an 8-bit number

	Set 1	Set 2
DATA 2501	96H	E4H
RESULT 2502	6AH	1CH

(d) 2's complement of a 16-bit number

	Set 1	Set 2
DATA 2501	8CH	00H
DATA 2502	5BH	5BH
RESULT 2503	74H	00H

	Set 1	Set 2
RESULT 2504	A4H	A5H

Conclusion

The program is executed and the results are stored in the memory locations.